MEK68I0

INPUT/OUTPUT INTERFACE BOARD

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INTRODUCTION

This manual describes the MEK68I0 which is a general purpose Input/Output Interface board for expansion of MOKEP systems. The MEK68I0 can support a variety of serial and parallel I/O devices such as printers, ASCII terminals, or current loop devices. In addition it can support mass storage and recovery of programs or data on an audio cassette recorder.

This manual describes how the MEK68I0 works and how it could be connected to some of these devices.

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CHAPTER 1

DESCRIPTION AND OPERATION

1.0 General Description

The MEK68I0 is a multi-use Input/Output Interface board for MOKEP system expansion. In it's basic configuration it can support record and play-back of 300 or 1200 baud cassette tapes, an RS-232 compatible serial port at baud rates of 110 to 9600, and an uncommitted PIA port for parallel interface.

The MEK68I0 has been designed to accept several user supplied options, which include the following:

a) An additional PIA port.

b) An additional RS-232 port.

c) A 20 mA current loop (TTY) interface.

d) A MIKBUG II type cassette interface.

e) An IEEE-488 instrumentation bus interface.

The MEK68I0 can be memory mapped in any one of four locations thus allowing up to four I/O boards to co-exist in an expanded system.

1.1 Address Space

The MEK68I/0 board occupies twenty addresses. These addresses were selected so as not to conflict with any of the other MOKEP boards. By use of jumper options, the base address for the I/0 board may be moved to any of four locations in the memory map so that up to four I/0 boards may co-exist in the same system. Table 1.1 shows the possible locations of the I/0 board in the system memory map.

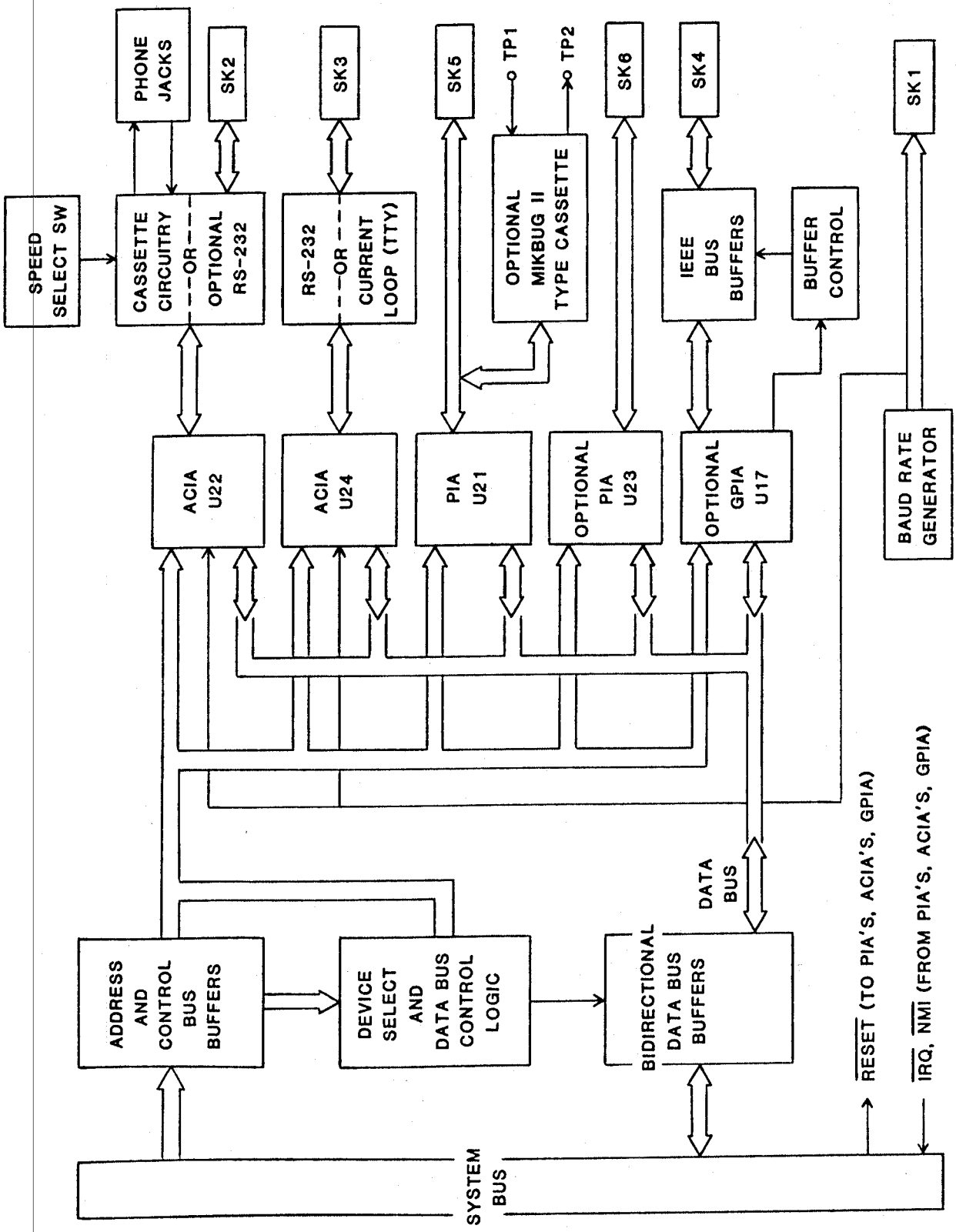

FIGURE 1.1. SYSTEM BLOCK DIAGRAM

1.1 Address Space (cont'd)

TABLE 1.1. ADDRESS SELECTION

Option	Decoded Base Location					Jumpers			
	PIA (U23)	PIA (U21)	ACIA (U24)	ACIA (U22)	GIPA (U17)	E13	E14	E12	E11
1	8000	8004	8008	800A	8048	No	Yes	No	Yes
2	8010	8014	8018	801A	8058	No	Yes	Yes	No
3	8020	8024	8028	802A	8068	Yes	No	No	Yes
4	8030	8034	8038	803A	8078	Yes	No	Yes	No

Boards are normally shipped in the option 1 configuration. See jumper section for details on relocating the board in the memory map.

Each PIA takes up to 4 ADDR locations.

Each ACIA takes up to 2 ADDR locations.

The GPIA takes up to 8 ADDR locations.

The MEK68IO has control of the bus for all 20 addresses, even if the peripheral parts are not in place.

1.2 Cassette Operation

A common audio cassette recorder may be used in conjunction with operating system firmware to add cassette mass storage to your MOKEP system. Description of operating system firmware is specifically omitted here as it depends on the firmware configuration (refer to the operating system manual for your system).

To connect your cassette recorder to the MEK68IO, run a cable from the

1.2 Cassette Operation (cont'd)

"MIC" input of your recorder to J1 on the I/O board and another from the "EAR" output of your recorder to J2 on the I/O board. Select your data rate (300 or 1200 baud) with switch S1. A detailed description of the cassette circuitry is found in section 2.1.

1.3 RS-232 Interface Operation

A standard RS-232 compatible device may be connected to your I/O board to expand the capabilities of your MOKEP system. In most cases you will have to supply firmware or software to support these devices, therefore the necessary address access information is supplied here.

The heart of this interface is an MC6850 Asyncronous Serial Interface Adaptor (ACIA, U24). MC1488 drivers and MC1489 receivers are used to translate logic levels. The following signals are used to accomplish the interface:

RXD - Receive Data

TXD - Transmit Data

RXCLK - Receive Clock

TXCLK - Transmit Clock

$\overline{\text{RTS}}$ - Request-to-Send

$\overline{\text{CTS}}$ - Clear-to-Send

$\overline{\text{DCD}}$ - Data Carrier Detect

The following step-by-step procedure should results in proper connection of your RS-232 device.

1) Determine the requirements for the $\overline{\text{DCD}}$ and $\overline{\text{CTS}}$ handshake controls.

1.3 RS-232 Interface Operation (cont'd)

In many cases your RS-232 device will not provide logic to drive these lines (nor require it for that matter), however the ACIA requires that they be a logic "Ø" in order to operate. If this is the case, then on your interface connector (mates with SK3), connect jumper pins 4 and 16 ($\overline{DCD}$ and $\overline{CTS}$) to pin 2 (GND).

2) Determine your requirements for $\overline{RTS}$. This ACIA output is program controllable and is sometimes used as a device control (i.e., Reader On). If this is not required, then proceed to step 3.

For the user's convenience, $\overline{RTS}$ is available in three different forms. When you have selected the desired form, check to make sure that only one of: E15, E16, or R35 is installed or you will have conflicting outputs tied together.

a) Direct from the ACIA, 0 to 25 volt logic. Select option "a" by installing E15 jumper.

b) Interfaced for $\pm$12 volt logic swing. Select option "b" by installing E16 jumper.

c) Interfaced for current loop compatibility. Select option "c" by installing R35, R34, and U15.

3) Determine your requirements for RXCLK and TXCLK clock rates (baud rate). A MC14411 baud rate generator (U3) is provided to supply a wide range of frequencies compatible with the ACIA. To select a clock frequency, connect jumpers on SK1 to route the appropriate frequencies to the ACIA

inputs. The MC14411 is hard wired for 16x mode, so that the actual frequencies are 16 times the baud rate (refer to Table 1.2). When you write your software, set-up the ACIA for 16x mode.

TABLE 1.2. BAUD RATE vs FREQUENCY

Outputs Drive RXCLK and TXCLK Inputs Only			
Baud Rate	SK1 Pin #	Nominal Frequency	Units
110	13	1758.8	Hz
300	7	4800.0	Hz
600	5	9600.0	Hz
1200	4	19.2	KHz
2400	3	38.4	KHz
3600	16	57.6	KHz
4800	2	76.8	KHz
9600	1	153.6	KHz
AUXILIARY/XTAL ÷ 2	SK1 Pin #	Nominal Frequency	Units
921.6 KHz	18	921.6	KHz

4) RXD is the 0 to 5 volt level logic input to the ACIA and is available for connection of various translators. In the case of an RS-232 device, we need ±12 volt logic swings. Receiver U4A (MC1489) performs the required translation. Connect a jumper from SK3 pin 15 to SK3 pin 14 and connect the incoming data from your RS-232 device to SK3 pin 1 (RS-232 IN).

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MEK68IO INPUT/OUTPUT BOARD CORRIGENDUM

Please make the following corrections to the MEK68IO Manual.

Page 1-6 Replace Table 1.2 with:

TABLE 1.2. BAUD RATE vs FREQUENCY

Outputs Drive RXCLK and TXCLK Inputs Only			
Baud Rate	SK1 Pin #	Nominal Frequency	Units
110	16	1758.8	Hz
300	15	4800.0	Hz
600	14	9600.0	Hz
1200	13	19.2	KHz
2400	12	38.4	KHz
3600	11	57.6	KHz
4800	10	76.8	KHz
9600	9	153.6	KHz
AUXILIARY/XTAL - 2	SK1 Pin #	Nominal Frequency	Units
921.6 KHz	8	921.6	KHz

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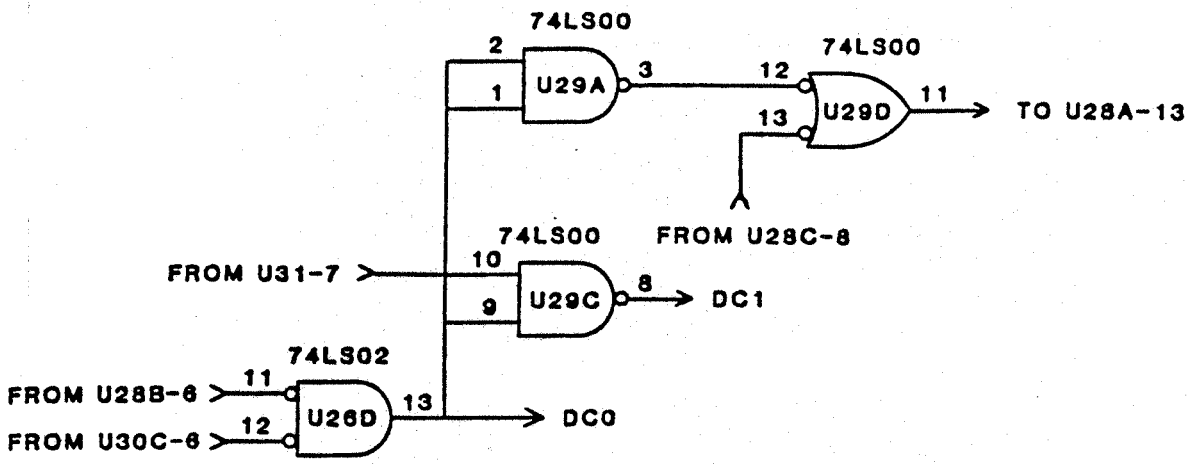
CORRIGENDUM (cont'd)

Appendix 3 Add U29A to System Schematic, sheet 2 (zone F6 and G6).

Also, remove U29A from Spares on System Schematic, sheet 3.



1.3 RS-232 Interface Operation (cont'd)

Note: The nomenclature for signals RXD and TXD, as given for some RS-232 devices, is confusing. Some manufacturers interpret "Receive Data" as meaning received by the device, while others interpret it as meaning receive for the processor. The MEK68I0 considers RXD to be data incoming to itself and TXD to be data outgoing to the RS-232 device. Damage may result from the accidental misconnection of these two signals and the system will not operate correctly.

5) TXD is the 0 to 5 volt logic data output from the ACIA and is available for connection of various translators. In the case of an RS-232 device, we need ±12 volt logic swings. Driver U5A (MC1488) performs the required translation. Connect a jumper from SK3 pin 11 to SK3 pin 12 and connect SK3 pin 3 to the outgoing RS-232 data line to your RS-232 deivce.

6) Connect your RS-232 data common lines, as necessary, to SK3 pin 2.

7) If you require +12 volts or -12 volts, you may connect to SK3 pins 5 and 7 as required.

8) You are now ready to write your software to drive your RS-232 device. The applicable addressing information is as follows:

(U24) ACIA Data Register $8008*

(U24) ACIA Status/Control $8009*

*Recall options allow relocation, see Table 1.1.

a) Normally you will set the ACIA to operate in 16x mode.

1.3 RS-232 Interface Operation (cont'd)

b) Refer to MC6850 for programming information.

c) D3BUG2 firmware provides for RS-232 operation and senses the existence of the RS-232 device by sensing the absence of the E5 jumper.

1.4 Parallel Interface Operation

The MEK6810 has the ability to interface with parallel I/O devices through SK5. A great deal of flexibility is allowed by the MC6821 PIA which forms the heart of this parallel port.

Note: In addition to serving this port, PIA U21 also serves the optional MIKBUG II cassette and a configuration sense bit. The configuration sense bit is a bit which can be sensed by the program. The D3BUG2 expansion firmware uses this bit to decide whether the user has an RS-232 terminal instead of an MEK68R2M Video Display board. If the firmware sees a "Ø" (normal configuration), it assumes it is to use an R2M board as the system console device and if it sees (senses) a "1", it assumes it is to use an RS-232 terminal as the system console. In general this would render the A-side port of the PIA addressed at $8ØØ4 unusable for other purposes. You will have to review the restrictions imposed by your particular firmware configuration, but the following guidelines should help:

1) If you wish to use the MIKBUG II cassette circuitry. U21 must be present and the A-side port at SK5 should not be used as a general purpose port.

2) If you have D3BUG2 expansion firmware and wish to use an RS-232 ter-

minal as your console device, U21 must be present, you must have an RS-232 terminal connected at SK3, the MEK68IO must have its base address (E11, E12, E13, and E14) in the "Normal" configuration, and J5 jumper trace must be cut. In this situation, the A-side port at SK5 should not be used as a general purpose port.

3) If you have D3BUG2 expansion firmware and are using an R2M board as your system console device, the PIA at U21 may be removed and placed in U23. The firmware will recognize the lack of a PIA at U21 and assume R2M operation and you will have a totally uncommitted PIA port available at SK6. An alternate way is to leave the PIA in U21 and just not use the A-side port as a general purpose port.

4) If you do not have D3BUG2 expansion firmware and wish to use the A-side port at SK5, you can remove R31 and cut the jumper trace E5. Check to be sure none of E4, E6, or E7 are installed and you may now use the A-side port at SK5 as you wish.

5) If you change the base address of the MEK68IO (with jumpers E11, E12, E13, and E14) the firmware no longer accesses it so R31 could be removed and E5 cut to totally free up the SK5 A-side port. Note that in order to use D3BUG cassette, you must have one MEK68IO with its base address set up to the normal configuration.

In addition to twenty PIA interface lines, SK5 allows connection to the system $\overline{IRQ}$ (Interrupt Request) and $\overline{NMI}$ (Non-Maskable Interrupt) lines.

1.4 Parallel Interface Operation (cont'd)

Any device connected to these lines must be an "open-collector" or an "open-drain" type device which signals a request for service by presenting the low impedance to the line and signals a lack of activity by presenting the appearance of no connection, thus allowing any other interrupting device on the same line to gain control.

The following is a brief description of the PIA interface lines (refer to the MC6821 data sheet for a more detailed discussion).

PAØ through PA7 - Eight peripheral interface lines which can be programmed independently as inputs or outputs.

PBØ through PB7 - Eight peripheral interface lines which can be programmed independently as inputs or outputs.

CA1 and CB1 - These control inputs can be programmed to cause an interrupt on positive or negative going edges and the interrupt may be masked from causing a system $\overline{IRQ}$.

CA2 and CB2 - These control bits may be programmed as inputs or outputs. Like CA1 and CA2, when they are programmed as inputs they may be set-up to respond to positive or to negative edges. When programmed as outputs, they can be set-up to act as read strobe, write strobe, or behave as an additional latched output bit.

The following addressing information will help in programming the parallel ports:

1.4 Parallel Interface Operation (cont'd)

TABLE 1.3. PIA ADDRESSING

		Base Address Option (TABLE 1.1)			
		1	2	3	4
U23 PIA (SK6)	Data Reg A*	$8000	$8010	$8020	$8030
	Data Direction A*	$8000	$8010	$8020	$8030
	Status/Control A	$8001	$8011	$8021	$8031
	Data Reg B*	$8002	$8012	$8022	$8032
	Data Direction B*	$8002	$8012	$8022	$8032
	Status/Control B	$8003	$8013	$8023	$8033
U21 PIA (SK5)	Data Reg A*	$8004	$8014	$8024	$8034
	Data Direction A*	$8004	$8014	$8024	$8034
	Status/Control A	$8005	$8015	$8025	$8035
	Data Reg B*	$8006	$8016	$8026	$8036
	Data Direction B*	$8006	$8016	$8026	$8036
	Status/Control B	$8007	$8017	$8027	$8037

* Besides the address select, control register bit 2 is required to determine whether the port or the data direction register will be accessed.

CR Bit 2 = 0 ⟶ Select Data Direction

CR Bit 2 = 1 ⟶ Select Data Reg (Port)

1.5 User Supplied Options

In addition to those features described above the I/O board has been

laid out to allow the user to easily implement some other options.

1.5.1 TTY (Current Loop) Option

In order to use the current loop option, the user must supply the following components:

TABLE 1.4. CURRENT LOOP COMPONENTS

Quanity	Description	Symbol
3	4N33 Opto-coupler	U14, U15*, U16
2	1N4002 Diode	CR3, CR4
1	1.0 uf Capacitor	C21
1	150 ohm, 1W Resistor	R35*
1	620 ohm, 1/4W Resistor	R18
1	820 ohm, 1W Resistor	R36
1	1.1K, 1W Resistor	R33
2	2.2K, 1W Resistor	R25, R34*
1	39K, 1/4W Resistor	R27

* Required only if AUX $\overline{\text{RTSY}}$ control (Reader On) desired.

Connections are made as shown in Figure 1.2.

Connect jumper from SK3 Pin 13 (RD) to SK3 Pin 14 (RXD), connect jumper from SK3 Pin 11 (TXD) to SK3 Pin 10 (TD) and use header at SK1 to program the baud rate. Pins 1 & 2 (TXCLK, RX CLK) must be connected to one of the baud rates (Pins 16-9).

1.5.1 TTY (Current Loop) Option (cont'd)

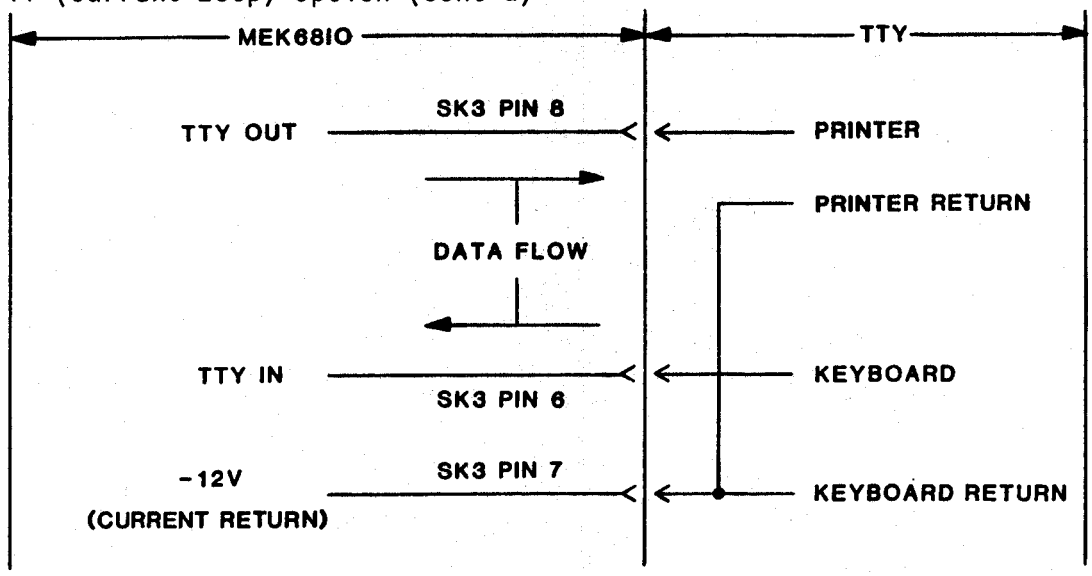


FIGURE 1.2. CONNECTION DIAGRAM

Note: The SK3 port cannot be used as both an RS-232 port and a current loop port at the same time, but SK2 could be used as an RS-232 port while SK3 is being used as a current loop port.

The ACIA addresses are:	Data	$8ØØ8
	Status/control	$8ØØ9

1.5.2 MIKBUG II Cassette Option

In order to use the MIKBUG II cassette option, the user must supply the components shown in Table 1.5.

The "Audio In" from your cassette is connected between TP1 and GND, and the "Audio Out" to your cassette is connected between TP2 and GND. PIA U21 services this option and may be addressed at $8ØØ4 (Data) and $8ØØ5 (Status/Control). "Audio In" is available at PAØ and "Audio Out" is in PA2.

1.5.2 MIKBUG II Cassette Option (cont'd)

TABLE 1.5. MIKBUG II CIRCUIT COMPONENTS

Quanity	Description	Symbol
1	MC14583 Dual Schmitt Trigger	U25
1	.1 uf capacitors	C34
2	zero ohm jumpers	E4, (E6 or E7)*
1	470 ohm, 1/4W resistor	R29
1	4.7K, 1/4W resistor	R30
1	22K, 1/4W resistor	R28
1	100K, 1/4W resistor	R32

* A zero ohm jumper is required at E6 if inverted data in is desired or at E7 if un-inverted data in is desired.

1.5.3 GPIA Option

For those wishing to evaluate the IEEE instrumentation bus interface, the MEK6810 has been designed to allow easy implementation of a circuit which can perform this function. In order to use this option, the user must supply the following components:

TABLE 1.6. MIKBUG II CIRCUIT COMPONENTS

Quanity	Description	Symbol
1	MC68488 GPIA	U17
4	MC3448 Bus Transceiver	U6, 7, 10, 11
1	24-Pin DIP socket	SK4

Refer to schematics for pin-outs on SK3.

CHAPTER 2

HARDWARE DESCRIPTION

2.0 Data Bus Decode Logic

The data bus direction is controlled by the "RDEN" signal into the enable inputs of data buffers U32 and U33. When RDEN is high, the buffer sections driving the system bus are enabled (Processor Read). When RDEN is low, the buffer sections driving the board from the system bus are enabled (Processor Write or Board not selected). RDEN (U27-4) results from the logical combination of "E" (U28-1), "R/$\overline{W}$" (U28-2), and "Board Select" (U28-13). "Board Select", in turn, is the logical combination of "$\overline{DC\emptyset}$" (U29-13) or "GPIAS" (U29-12). GPIAS is valid for an access to any of the eight GPIA addresses and $\overline{DC\emptyset}$ is the logical combination of A6 and "BASE ADDRESS". "BASE ADDRESS" can be any of the four possible combinations of A4 and A5 combined with "I/O1" which is decoded on the CPU board to be $8000-$807F. Table 2.1 summarizes the decoding logic.

2.1 Cassette Circuitry

The bulk of the circuitry on the MEK68IO is related to the cassette circuitry. The interface to the MOKEP system is handled by an MC6850 ACIA (22) and a more detailed description concerning its operation can be found in the MC6850 data sheet (see Appendix 1). The major functional blocks within the cassette circuitry are:

1. Data generation (U9A and U9B).
2. Wave shaping (U2C).
3. Data recovery (U2A, U2B, U13, and U20).

TABLE 2.1. DECODE LOGIC SUMMARY

Device	U#	E	R/$\overline{W}$	I/O1	A6	A5	A4	$\overline{DC0}$	$\overline{DC1}$	$\overline{GPIAS}$	A3	A2	A1	A0	"Normal Address"
PIA	U23	1	X	1	0	*	*	1	1	1	0	0	X	X	$8000-8003
PIA	U21	1	X	1	0	*	*	1	1	1	0	1	X	X	$8004-8007
ACIA	U24	1	X	1	0	*	*	1	0	1	1	0	0	X	$8008-8009
ACIA	U22	1	X	1	0	*	*	1	0	1	1	0	1	X	$800A-800B
GPIA	U17	1	X	1	1	*	*	0	1	0	1	X	X	X	$8048-804F

X = Don't care.

I/O1 = A15 • $\overline{A14}$ • $\overline{A13}$ • $\overline{A12}$ • $\overline{A11}$ • $\overline{A10}$ • $\overline{A9}$ • $\overline{A8}$ • $\overline{A7}$ • VMA (i.e., $8000-807F).

I/O1 must be high (true) for any device to be selected.

RDEN = High (processor read) for E • R/$\overline{W}$ • (any device selected).

Low all other times (data active direction toward board).

* A5, A4 - Select the board's basic address:

Option 1 - $\overline{A5}$ • $\overline{A4}$ - E14 • E11 • $\overline{E13}$ • $\overline{E12}$ - "Normal" option

2 - $\overline{A5}$ • A4 - E14 • E12 • $\overline{E13}$ • $\overline{E11}$

3 - A5 • $\overline{A4}$ - E13 • E11 • $\overline{E14}$ • $\overline{E12}$

4 - A5 • A4 - E13 • E12 • $\overline{E14}$ • $\overline{E11}$

2.1 Cassette Circuitry (cont'd)

4. Clock recovery (U18, U12, and U8).

5. Data rate select (S1 and U1).

2.1.1 Data Generation

Transmit data from the ACIA must be converted to a wave train of 1200 and 2400 Hz signals. A data value of "Ø" is converted to four cycles of 1200 Hz and a data value of "1" is converted to eight cycles of 2400 Hz corresponding to a "Bit Time" of 3.33 ms for 300 baud data rate. If 1200 baud is selected, the logic equivalents would be: "0" - 1 cycle 1200 Hz; "1" - 2 cycles 2400 Hz corresponding to a bit time of .8325 ms.

This conversion is performed by J-K flip-flop sections U9A and U9B, which are connected to act as divide-by-two stages. A 4800 Hz signal from the MC14411 baud rate generator (Pin 7, 300 baud x 16 = 4800 Hz) is buffered by U19F and drives the clock inputs of the divide-by-two stages. Inverted transmit data from the ACIA controls U9A such that if TXD = "1"; the preset, J, and K inputs to U9A will be low thus disabling that stage and presenting a logic "1" to the J and K inputs of U9B. The end result is:

If TXD = "Ø" both U9A and U9B divide-by-two, making U9B pin 9 be 4800 Hz divided by four or 1200 Hz.

If TXD = "1" U9A will be disabled and only U9B will divide-by-two, making U9B pin 9 be 4800 Hz divided by two or 2400 Hz.

2.1.2 Wave Shaping

The signal produced at U9B pin 9 is the right frequency but is a square

2.1.2 Wave Shaping (cont'd)

wave with little drive capability. U2C acts as a buffer to "Square-Up" the TTL output at U9B Pin 9. The passive network made up of C3, R1, R2, and C2 shapes the waveform to make it look more like an audio sine wave. The network also attenuates the signal by a factor of 100:10,000 or 1:100 so that the output signal is approximately 50 mV p-p. This signal is now suitable to drive a "MIC" input on a common cassette recorder. The frequency response of the tape itself will further shape the audio signal by rounding the sharp corners at the peaks.

2.1.3 Data Recovery

Data recovery circuitry must distinguish the difference between a 1200 Hz half cycle (417 us) and a 2400 Hz half cycle (208 us) and present this data to the receive data input of the ACIA. U2A amplifies the incoming audio signal from the "EAR" phone jack to "SQUARE" it up. U2B acts as a peak detector, generating a pulse for each change in polarity of the incoming signal. U13A is used to clean up and buffer the pulses coming from U2B pin 4. For each positive logic transition at U13A pin 4, a postive going square pulse about 100 us long will be generated at U13A pin 6. The connection from U13A pin 7 to pin 5 makes this one-shot stage non-retriggerable which makes the system immune to noise until U13A has timed-out. U13B is used as a discriminator to decide whether pulses are spaced at 1200 Hz half cycles or 2400 Hz half cycles.

This one-shot (U13B) is set to time out at about 270 us and is retriggered each time a rising edge appears at U13B pin 12. If the incoming audio

2.1.3 Data Recovery (cont'd)

signal is 2400 Hz, pulses at U13B pin 12 will be approximately 208 us apart so U13B will always be retriggered and never time out (U13B pin 10 will always be high). If the incoming audio signal is 1200 Hz, pulses at U13B will be spaced about 416 us apart which will now allow U13B to time out between triggers. The circuitry driving U20 contains some subtleties, but basically behaves as a shift register. The "shift-right" control is the rising edge of U13A pin 6 buffered through U19E to the clock inputs of U20. Assuming a continuous 2400 Hz input signal, a logic "1" at U20A pin 2 would appear at U20B pin 9 two half cycles later. Assuming a continuous 1200 Hz input signal, about 270 us into a half cycle, U13B will time-out causing U20A pin 1 to go low which will cause U20A pin 5 to go low immediately thus bypassing the shift requirement. This difference between the propigation requirements of a "1" vs a "Ø" is responsible for the circuitry's ability to ignore an accidental glich in the incoming data in the following manner.

Again assume a continuous incoming signal of 1200 Hz (corresponding to a bit value of "Ø"). U20B pin 9 which is connected to the receive data input of the ACIA will be low. Now assume a noise glich gets in and appears as a half cycle of some higher frequency. This will retrigger U13B so that when the next half cycle pulse comes (probably on the real 1200 Hz half cycle boundry) a logic "1" will shift from U20A pin 2 to U20A pin 5. Unless another glitch comes, the normal 1200 Hz half cycle will allow U13B to time out at about 270 ms into it. As soon as the time out occurs, U20A pin 1 (CLR) will go low destroying the invalid logic "1" state at pin 5

2.1.3 Data Recovery (cont'd)

before a second half cycle edge could transfer it to U20B pin 9 where the ACIA could see it.

The data recovered by the above described circuitry is presented to the "Receive Data" input (RXD) of the ACIA.

2.1.4 Clock Recovery

Due to the asynchronous nature of the cassette media it is necessary to derive the data clock from the incoming audio signal in order to assure synchronization with the recovered data. U18B is used to recover a constant 2400 Hz clock reguardless of the data content of the incoming signal. U18B is connected as a flip flop which changes state on each positive going edge on U18B pin 11 and is asynchronously cleared on each time out of U13B. Since the initial logic state of U18B is not known, some means of synchronization is required before we can discuss its subsequent behavior. The incoming audio signal is required to have a leader which contains both logic frequencies. As soon as a valid 1200 Hz half cycle has been detected, U18B pin 8 is forced high by a U13B time out. From this point on U18B is synchronized such that the rising edge at U13A pin 6 which marks the beginning of any 1200 Hz half cycle will result in U18B pin 8 going low and the subsequent time out of U13B pin 10 will cause a pulse on U18B pin 10 causing U18B pin to return high. Within any 1200 Hz half cycle of audio coming in there will be one full cycle of simulated 2400 Hz at U18B pin 8. When the incoming audio is 2400 Hz, there is no activity on U18B pin 10 and U18B simply changes state at each 2400 Hz

2.1.4 Clock Recovery (cont'd)

half cycle which produces a 2400 Hz square wave at U18B pin 8. Since the duty cycle at U18B pin 8 is not 50% during recovery of logic "Ø" data, U18A is connected as a divide-by-two to correct this phase deviation and a 1200 Hz 50% duty cycle square wave results at U18A pin 6. A phase lock loop (U12) is used to compensate for tape speed variations and to multiply this recovered clock to arrive at the 16x clock frequency required for the ACIA. U8 is used as a divider in the feedback loop of the phase lock loop to achieve the required multiplication factor.

2.1.5 Data Rate Select

The multiplexer (U1) is used to route the proper frequencies to the TXCLK and RXCLK of the ACIA for either 300 or 1200 baud data rates. When S1 is in the 300 baud position, U1 routes the signal from pin 4 to TXCLK (pin 7) and from pin 12 to RXCLK (pin 9). When S1 is in the 1200 baud position, U1 routes the signal from pin 5 to TXCLK (pin 7) and from pin 11 to RXCLK (pin 9).

2.2 Serial Interface Ports

There are two serial interface ports on the MEK68I0 which can be configured by the user to serve a wide variety of serial peripherals in various combinations. One of the ACIA's serving these ports is normally used by the cassette circuitry, but can be freed for independent use at the expense of the cassette capability.

2.2.1 Baud Rate Generator

An MC14411 baud rate generator is provided to supply signals suitable for

2.2.1 Baud Rate Generator (cont'd)

use as RXCLK's and TXCLK's for the ACIA's. Y1 provides a stable 1.8432 MHz source which is divided down by U3 to arrive at the various baud rates. RSA is tied low and RSB is tied high to put U3 in the 16 times mode so the frequencies present at the baud rate outputs are actually 16 times the baud rate (see Table 1.2).

2.2.2 RS-232

Either SK2 or SK3 may be reconfigured as RS-232 compatible ports (see section 1.3). MC1488 sections translate 0 to 5 volt logic level signals to RS-232 compatible signals and MC1489 sections translate RS-232 compatible signals into 0 to 5 volt logic level signals for use by the ACIA.

2.2.3 Current Loop

SK3 can be configured to serve as a 20 mA neutral current loop port (see section 1.5.1). Transmitted data leaves U24 pin 6 and is routed, via a user supplied jumper from SK3 pin 11 to SK3 pin 10, to U5C pins 9 and 10. U5C translates the 0 to 5 volt logic levels to $\pm$12 volt logic levels, which are then presented to the primary side of the optical-coupler (U16). U16 provides the necessary gain to drive the 20 mA current loop at SK3 pin 8. The current return point is -12 volts at SK3 pin 7. Receive data present in the current loop connected between SK3 pin 6 and SK3 pin 7 (return) drives U14 primary side. Optical-coupler U14 translates loop current data to a $\pm$12 volt logic level data which is in turn presented to U4B pin 4 which further translates it to a 0 to 5 volt logic level data suitable for presentation to the receive data input of the ACIA. The

2.2.3 Current Loop (cont'd)

final link is supplied through a jumper from SK3 pin 13 to SK3 pin 14.

2.3 Parrallel Interface Ports

SK5 and SK6 are used as parallel interface ports, with the exception of $\overline{IRQ}$ and $\overline{NMI}$, the operation of these ports is solely governed by the MC6821 PIA's. For the detailed operation of a PIA, refer to the MC6821 data sheet located in Appendix 3.

Care should be exercised in using the $\overline{IRQ}$ and $\overline{NMI}$ inputs to SK5 and SK6 as these lines are not buffered on the MEK68I0. Any device connected to these lines should be of the "open-collector" or "open-drain" variety so as not to interfere with the ability of other devices to gain control. Long lines should be avoided as they may allow noise to enter the MOKEP system and cause erroneous interrupts.

CHAPTER 3

SIGNAL DESCRIPTIONS

3.0 Bus Signal Descriptions

The MEK68I0 board contains the following internal bus signals.

1) 7 address lines (AØ-A6) - For selection of one byte or location from 128 bytes or locations.

2) 8 data lines (DØ-D7) - Bidirectional lines that carry data information.

3) 6 control lines

   a) E (ENABLE) - This signal is the system clock. A standard 3.579549 MHz crystal is used by the processor to generate the 894.8 KHz system clock.

   b) R/$\overline{W}$ (Read/Write) - This is the read-write control line. It's logic state determines the direction of data (into or out of) a selected chip.

   c) VMA (Valid Memory Address) - When this control line is low, the address on the bus is not valid.

   d) $\overline{RESET}$ - This line is used to reset system devices.

   e) $\overline{IRQ}$ (Interrupt Request) - This signal requests that an interrupt sequence be generated within the processor.

   f) $\overline{NMI}$ (Non-Maskable Interrupt) - This signal is similar to $\overline{IRQ}$ except that the interrupt mask bit in the condition code register cannot be set to hold off or prevent an interrupt from being executed.

3.0 Bus Signal Descriptions (cont'd)

4) I/O1 select line - This select line is a logic "1" for the address space $8000 to $807F and a logic "0" for all other address combinations.

3.1 Bus Pin Assignments

The following table gives the bus pinout assignments for the MEK6810 board.

TABLE 3.1. SYSTEM BUS PINOUTS

Pin Number	Signal	Pin Number	Signal
1	GND	31	A1
2	E/02	32	A2
3	OPEN	33	A3
4	+5 V	34	A4
5	OPEN	35	A5
6	OPEN	36	A6
7	OPEN	37	OPEN
8	OPEN	38	OPEN
9	VMA	39	OPEN
10	OPEN	40	OPEN
11	R/$\overline{W}$	41	OPEN
12	GND	42	OPEN
13	$\overline{RESET}$	43	OPEN
14	$\overline{NMI}$	44	OPEN
15	$\overline{IRQ}$	45	OPEN
16	OPEN	46	GND
17	OPEN	47	GND
18	OPEN	48	D0
19	GND	49	D1
20	KEY SLOT	50	D2
21	OPEN	51	D3
22	OPEN	52	D4
23	OPEN	53	D5
24	OPEN	54	D6
25	OPEN	55	D7
26	OPEN	56	+12 V
27	I/O1	57	GND
28	OPEN	58	-12 V
29	OPEN	59	+5 V
30	A0	60	GND

3.2 Peripheral Interface Lines

The peripheral interface lines are described as follows:

1. Baud rate selection (SK1).
   a) Baud rates 110 thru 9600 (pins 9-16) are 16 times frequencies for driving the RX and TX inputs of an ACIA.
   b) RXCLK, TXCLK (pins 1, 2) are the receive and transmit clock inputs to U24 (ACIA).
   c) RXCLK, TXCLK (pins 3, 4) are the receive and transmit clock inputs to U22 (ACIA). E9 and E10 jumpers also connect the cassette circuitry to these points and must be removed prior to reconfiguring SK2 as an RS-232 port.
   d) 921.6 KHz is a user definable signal from which baud rates may be derived. It is one half the on board baud rate crystal frequency.

2. Serial Interface Ports (SK2, SK3)
   a) GND, +12, -12 (pins 2, 5, and 7 respectively) are connections to MOKEP power supplies commonly used for serial interface.
   b) $\overline{\text{RTSY}}$ - by use of E15, E16, and R35, this line can be:
      (1) $\overline{\text{RTS}}$ direct from ACIA (U24).
      (2) $\overline{\text{RTS}}$ interfaced for RS-232 compatibility.
      (3) $\overline{\text{RTS}}$ interfaced for current loop compatibility.
   c) $\overline{\text{RTS}}$ (Request-To-Send) - This ACIA output allows program control of modem or other peripheral device.
   d) $\overline{\text{CTS}}$ (Clear-To-Send) - This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link.

3.2 Peripheral Interface Lines (cont'd)

e) $\overline{DCD}$ (Data-Carrier-Detect) - This high impedance TTL compatible input provides automatic control of the receiving end of a communications link.

f) TXD - Transmit Data Output from ACIA.

g) RXD - Receive Data Input to ACIA.

h) RS-232 OUT - An RS-232 compatible output to an RS-232 device.

i) RS-232 IN - An RS-232 compatible input from an RS-232 device.

j) DATA IN - The digital data from the RS-232 device after it has been converted to be compatible with the RXD input to the ACIA.

k) DATA OUT - When digital data from the ACIA is presented to this input, it is converted to be RS-232 compatible and is made available at the RS-232 out pin.

l) TTY IN - Current loop compatible input from a TTY or other current loop device.

m) TTY OUT - Current loop compatible output to a TTY or other current loop device.

n) RD - ACIA RXD compatible signal which results from converting the TTY IN signal.

o) TD - When the ACIA TXD output is connected to this pin, the data is converted for current loop compatibility and presented on the TTY OUT pin.

3. Parallel Interface Lines (SK5, SK6)

a) +5, GND (pins 24 and 13 respectively) - These are connections to

3.2 Peripheral Interface Lines (cont'd)

the MOKEP power supplies.

b) NMI, IRQ (Pins 1 & 2) - These high impedance lines allow access to the systems interrupt lines. Only open-collector or open-drain devices may be connected to these lines. The MEK68I0 board does not buffer these lines prior to presenting them to the bus.

c) CA1, CB1 - These are programmable interrupt input control lines to a PIA.

d) CA2, CB2 - These are programmable PIA control lines which can be configured as inputs or outputs for a varity of handshake and peripheral control applications.

e) PAØ through PA7 - "A" side PIA parallel interface lines which may be configured as inputs or outputs in any combination under software control.

f) PBØ through PB7 - "B" side PIA parallel interface lines which may be configured as inputs or outputs in any combination under software control.

CHAPTER 4

SWITCHES AND JUMPERS

4.0 Switches

S1 is a cassette data rate select switch, which in conjunction with system software, allows the user to choose 300 or 1200 baud as the cassette data transmission rate.

4.1 Jumper Options

All normal jumper options are etched onto the PC board at the time of fabication. If the user wishes to change this configuration, he must first remove the unwanted connections by cutting the jumper traces and then install the new configuration by soldering in wire jumpers at the required locations.

A) Jumpers E1 and E2 allow the user to ground the $\overline{CTS}$ and $\overline{DCO}$ inputs to the ACIA (U22). In the normal configuration, U22 serves the cassette circuitry and both E1 and E2 are present.

B) E3 connects the ACIA (U22) transmit data to the cassette interface circuitry and is present in the normal configuration.

C) E4 is used to enable the audio output when using the MIKBUG II cassette option and is normally not present.

D) E5 is used to indicate to the system software, whether or not an RS-232 terminal is being used with the system. In the normal configuration, the jumper is present, indicating that RS-232 is not present.

E) E6 and E7 are used to connect data in from the optional MIKBUG II cassette circuit. If true data is desired, install E7, or if false

data is required, install E6. E6 and E7 should not both be present at any time. In the normal MEK68I0, neither E6 nor E7 are present.

F) E8 is used to connect the cassette input data to the RXD of ACIA U22, in the normal configuration E8 is present.

G) E9 is used to connect the recovered clock from the cassette circuit to the TXCLK input of ACIA U22 and is normally present.

H) E10 is used to connect the recovered clock from the cassette circuit to the RXCLK input of ACIA U22 and is normally present.

I) E11, E12, E13, and E14 are used to move the MEK68I0 to one of four possible locations in the system memory map. Table 1.1 shows how to use these jumpers. The normal configuration is option 1 with E11 and E14 present and E12 and E13 absent.

J) E15 and E16 are used along with R35 to select the method of interface for the RTS of ACIA (U24). Only one of the three devices should be installed at any time.

- E15 selects direct interface.
- E16 selects RS-232 compatible interface.
- R35 and associated circuitry selects current loop compatibility.

APPENDIX 1

DATA SHEETS

MC6821 PIA

MC6850 ACIA

MC68488 GPIA

APPENDIX 2

PARTS LIST

APPENDIX 2. PARTS LIST

Item Number	Quantity	Description	Part Number	Reference Designation
1	1	PC Board	MEK68I0	--
2	1	Integrated Circuit	74LS00	U29
3	1	Integrated Circuit	74LS02	U26
4	2	Integrated Circuit	74LS04	U27, U30
5	1	Integrated Circuit	74LS10	U28
6	2	Integrated Circuit	74LS74	U18, U20
7	1	Integrated Circuit	74LS112	U9
8	1	Integrated Circuit	74LS153	U1
9	3	Integrated Circuit	74LS241	U31 - U33
10	1	Integrated Circuit	MC3301	U2
11	1	Integrated Circuit	MC6821	U21
12	2	Integrated Circuit	MC6850	U22, U24
13	1	Integrated Circuit	MC14024/4024	U8
14	1	Integrated Circuit	MC14046	U12
15	1	Integrated Circuit	MC14050	U19
16	1	Integrated Circuit	MC14411	U3
17	1	Integrated Circuit	MC14538	U13
18	1	Integrated Circuit	MC1488	U5
19	1	Integrated Circuit	MC1489	U4
20	1	Crystal, 1.8432 MHz	NDK, CTS, Buck-Man	Y1
21	4	Resistor, 1.0 M 1/4 Watt, 5%		R5,R10,R12, R17
22	1	Resistor, 56K 1/4 Watt, 5%		R13

APPENDIX 2. PARTS LIST (cont'd)

Item Number	Quantity	Description	Part Number	Reference Designation
23	11	Resistor, 10K 1/4 Watt, 5%		R1,R4,R8,R9, R11,R14,R15, R16,R22,R31, R39
24	2	Resistor 100K 1/4 Watt, 5%		R20, R24
25	1	Resistor, 27K 1/4 Watt, 5%		R21
26	3	Resistor, 22K 1/4 Watt, 5%		R3, R6, R7
27	1	Resistor, 100 Ohm 1/4 Watt, 5%		R2
28	1	Resistor, 270K 1/4 Watt, 5%		R23
29	3	Socket, 16 Pin		SK1-SK3
30	5	Socket, 24 Pin		U3,U22,U24, SK5,SK6
31	2	Socket, 40 Pin		U21, U23
32	1	Capacitor, .005 uF Monolithic Ceramic		C52
33	3	Capacitor, 100 uF Aluminum Electrolytics		C42,C43,C44
34	1	Capacitor, 200 pF DM - Dipped Silver Mica		C18
35	2	Capacitor, .001 uF		C24, C25
36	1	Capacitor, .001 uF Monolithic Ceramic		C26
37	33	Capacitor, 0.1 uF Monolithic Ceramic		C1,C3,C4, C6-C8,C10,C12, C13,C16,C17, C19-C21,C27-C31,C33,C35-C41,C45-C47, C49-C51

APPENDIX 2. PARTS LIST (cont'd)

Item Number	Quantity	Description	Part Number	Reference Designation
38	1	Capacitor, 1 uF Monolithic Ceramic		C2
39	1	Key, Polarzing		(For P1)
40	1	Diode	1N914	CR1
41	1	Switch, Toggle, PC-SPDT		S1
42	6	Connector, 10 Pin		P1
43	2	Phone Jack		J1,J2
44	2	Mounting Bracket, Phone Jack		(For J1 & J2)
45	4	Screw, 4-40 x 5/16 PPH		(Ref only)
46	4	Nut, 4-40 Hex		(Ref only)
47	4	Washer, #4 Flat		(Ref only)

APPENDIX 3

SYSTEM SCHEMATIC

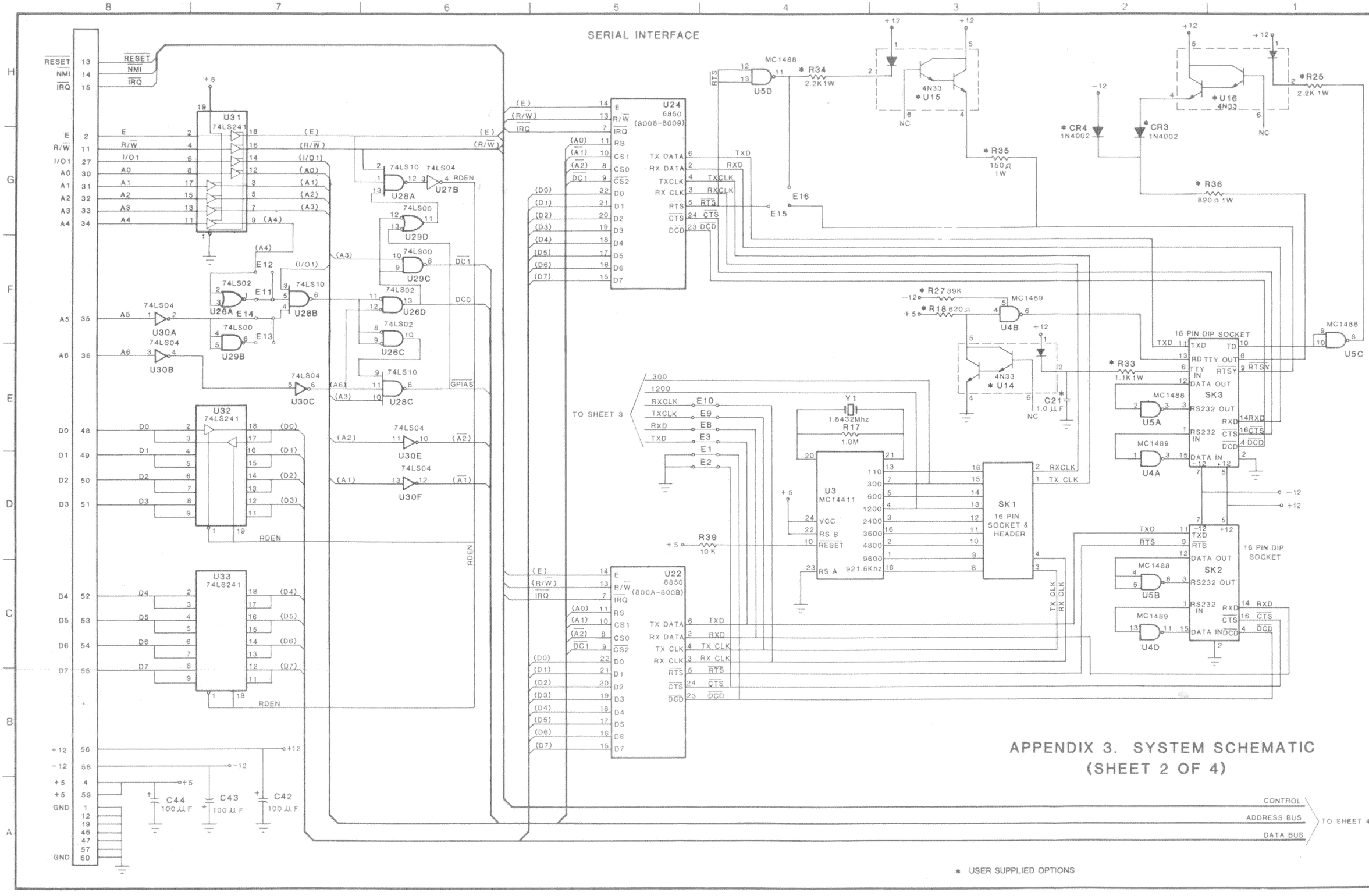
Sheet 1: Index Page

Sheet 2: System Schematic

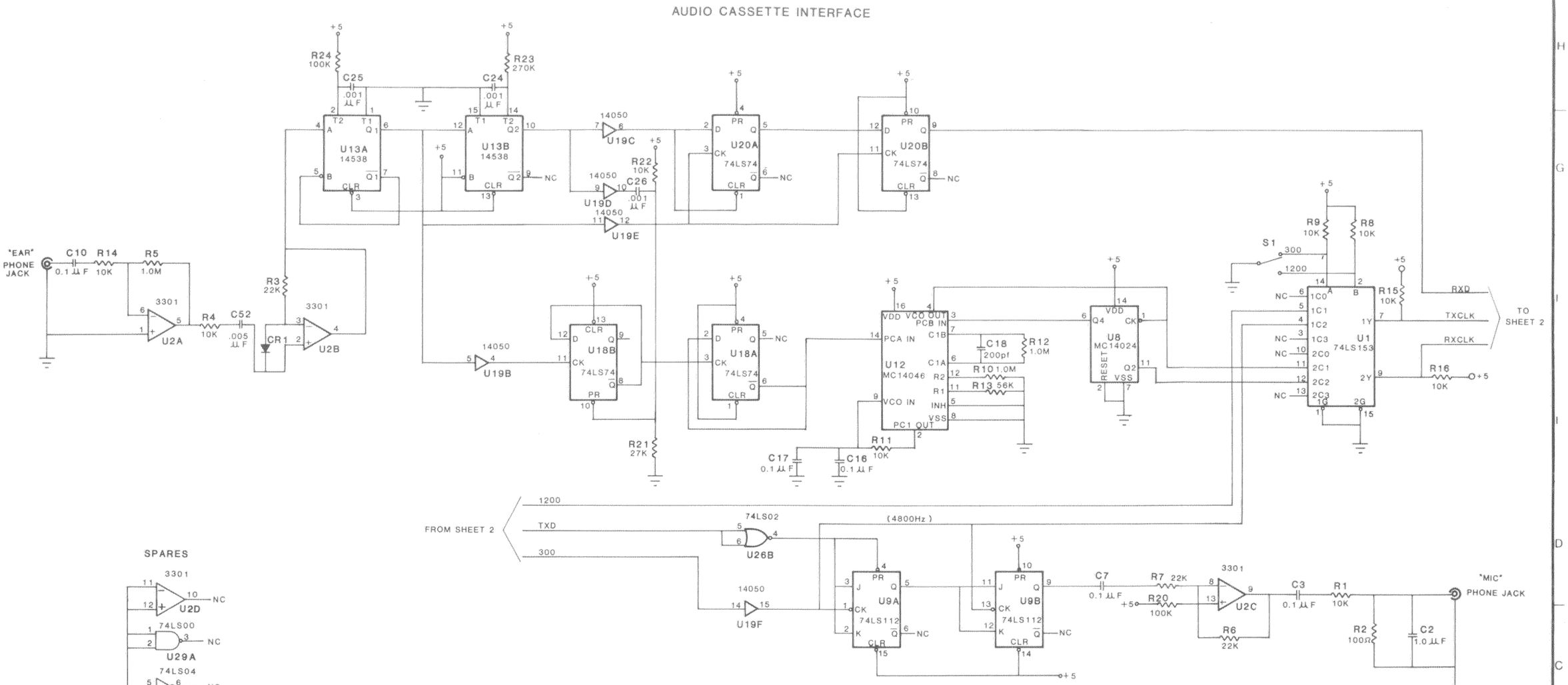
Sheet 3: System Schematic

Sheet 4: System Schematic

SERIAL INTERFACE



APPENDIX 3. SYSTEM SCHEMATIC (SHEET 2 OF 4)



POWER CONNECTIONS

DEVICE #	+5 PIN #	+12 PIN #	-12 PIN #	GND PIN #
U1, U6, U7, U9 - U13, U25	16			8
U5		14	1	7
U3	24			12
U2, U4, U8, U18, U20, U26- U30	14			7
U17, U21, U23	20			1
U19	1			8
U22, U24	12			1
U31 - U33	20			10

APPENDIX 3. SYSTEM SCHEMATIC (SHEET 3 OF 4)

RITTER CASSETTE INTERFACE

IEEE INTERFACE

*U25 MC14583

R31 10K

R32 100K

R30 4.7K

R29 470

R28 22K

C34 .1 U F

E4 E5 E6 E7

TP1 AUDIO IN

TP2 AUDIO OUT

SK5 24 PIN DIP SOCKET

SK6 24 PIN DIP SOCKET

SK4 24 PIN DIP SOCKET

U17 *MC68488

U21 6821 (8004-8007)

*U23 6821 (8000-8003)

*U6 MC3448

*U7 MC3448

*U10 MC3448

*U11 MC3448

74LS04 U27F

74LS04 U27E

FROM SHEET 2

CONTROL

ADDRESS BUS

DATA BUS

* USER SUPPLIED OPTIONS

APPENDIX 3. SYSTEM SCHEMATIC
(SHEET 4 OF 4)