MEK68RR

MOKEP ROM/RAM BOARD

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of this product described any license under the patent rights of Motorola, Inc., or others.

First Edition

Motorola, Inc., March 1979

TABLE OF CONTENTS

CHAPTER I

INTRODUCTION

1.0 General Description and Capability

The MEK68RR is a RAM/ROM module designed to be used with the D2/R2 kit combination or the MOKEP system.

The MEK68RR contains two RAM arrays and two ROM/EPROM sockets arrays. The RAM arrays use 2114 - 1K x 4 type RAMs, and are expandable to 4K bytes each. Each array may be mapped on any 4K boundary within the 65K memory map. The paging feature allows each RAM array to appear in one or more of eight pages. Each RAM array also has an independent write protect switch.

Each ROM array may be configured to accept 1K x 8, 2K x 8, 4K x 8, or 8K x 8 ROMs/EPROMs in either single voltage or 3 voltage types. Either array may occupy any part of the 65K memory map and may be paged in the same way as the RAM arrays.

1.1 Specifications

The specifications of the MEK68RR are outlined in Table 1.

1.2 Theory of Operation

The following paragraphs describe the theory of operation for the MEK68RR. Figure 1 is the overall block diagram.

The MEK68RR receives Address (AØ - A15), Paging (ROPØ-2, RAPØ-2), Enable (E), Read/Write (R/$\overline{W}$), Valid Memory Address (VMA), and Data (DØ - D7)

TABLE 1. CHARACTERISTICS AND SPECIFICATIONS

Characteristics	Specifications
Dimensions	
Width	8.25"
Height	7.00"
Board Thickness	0.062"
Power Requirements	+5 Vdc +12 Vdc -12 Vdc
RAM	2 arrays - Expandable to 4K bytes each (1K bytes provided)
ROM	2 arrays allowing use of 1K x 8, 2K x 8, 4Kx 8, or 8K x 8 ROMs/EPROMs
Input Signals	TTL voltage compatible (2 LS TTL loads Max)
Output Signals	Three - state LS TTL voltage compatible

1.2 Theory of Operation (cont'd)

signals from the bus. Each of these is received by a bus interface and applied to the appropriate area of the circuit.

The address lines are split into three groups: A12 through A15 are applied to the address mapping switches, AØ through A9 are applied to the ROM/EPROM array and the RAM array, and A10 through A11 are applied to the chip select decoders.

The memory address block, where each RAM array appears, is selected by the RAM address mapping switch. The RAM may be switched to any one of

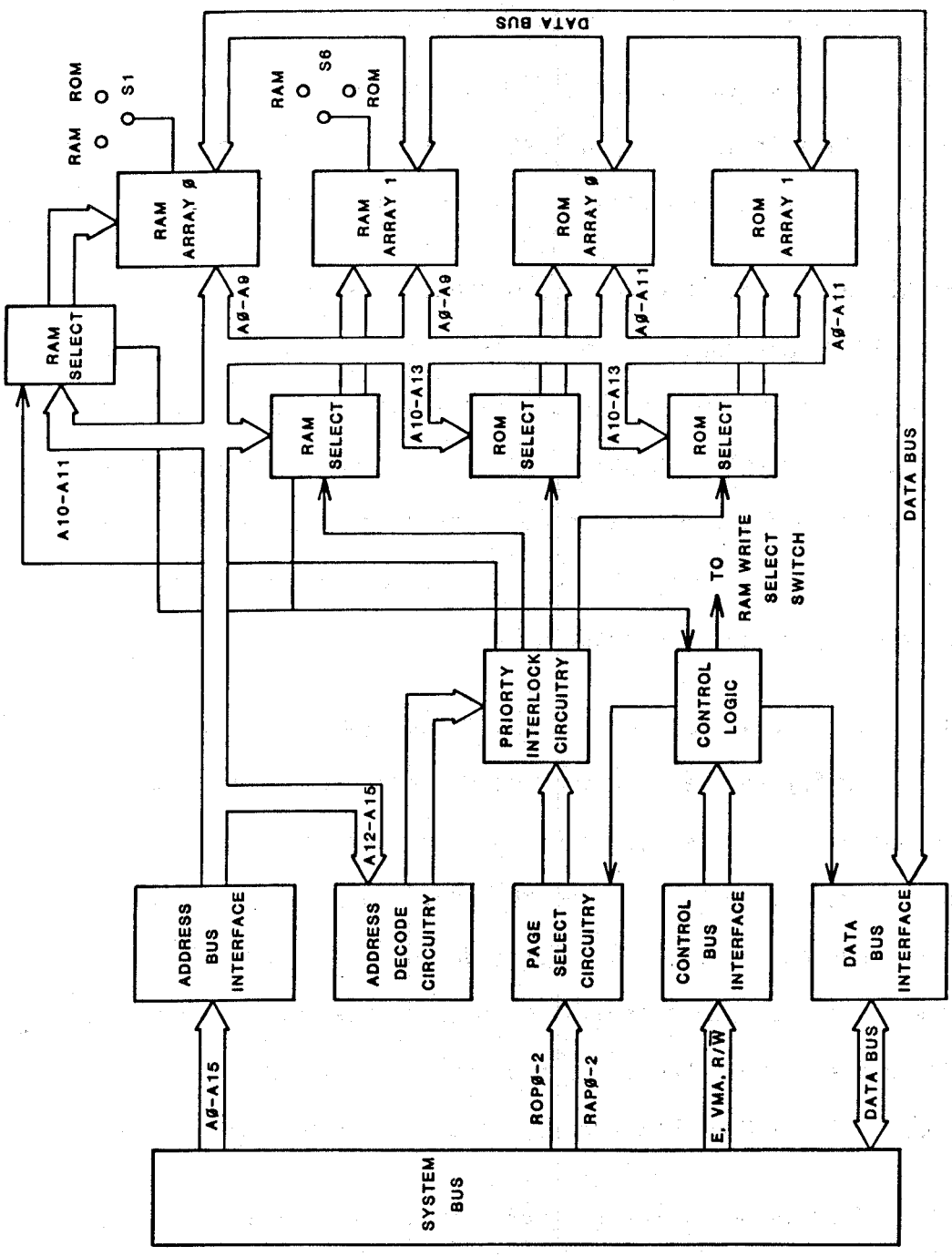


FIGURE 1. BLOCK DIAGRAM

1.2 Theory of Operation (cont'd)

sixteen 4K byte memory blocks. The RAM select circuit detects the desired combination of A12 through A15, and $\overline{A12}$ through $\overline{A15}$, enabling the RAM chip select decoder. A10 through A11 are used to determine which 2114's in the array are to be selected. AØ through A9 are used to select unique locations within individual RAM chips.

The ROM array select circuitry operates the same as the RAM when 1K x 8 ROMs/EPROMs are used. When larger size ROMs are used, provisions must be made to move some of the address lines from the chip select decoders to the ROM sockets. Also, different ROMs have various pinouts which require reconfiguring the sockets for different ROM/EPROM types. These conditions are accommodated by a series of jumper options and are described in detail in Chapter 2.

The MOKEP memory map includes 8 pages of RAM area and 8 pages of ROM area (see Appendix 4). Pages are selected by the page register on the CPU board. The page select signals (ROPØ-2 and RAPØ-2) are available on the bus and applied to the MEK68RR. Each set of signals is applied to an open collector, 3 to 1 of 8 decoder. The outputs of the decoder enter separate jumper arrays for each of the two RAM Arrays and the ROM arrays. There the individual page signals may be wired to allow a particular ROM or RAM array to appear in one or more pages.

Each RAM array has a write protect feature. Write protect is activated by positioning the RAM/ROM switch to the ROM position. The R/$\overline{W}$ signal is then gated high, and applied to the R/$\overline{W}$ line of the RAMs. The

1.2 Theory of Operation (cont'd)

priority interlock circuity prevents two RAM arrays or two ROM arrays from being simultaneously accessed when they map at the same address and the same page. Priority is given to RAM Array Ø and to ROM Array Ø.

CHAPTER 2

PREPARATION FOR USE

2.0 Unpacking

Unpack the MEK68RR Module from its shipping carton and, referring to the packing list, verify that all of the parts are present. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.1 Inspection

The MEK68RR Module should be inspected upon receipt and at periodic intervals. It is a good practice, however, to visually inspect the module when it is removed from the card cage. Inspect the module for broken, damaged, or missing parts and the printed circuit board for physical damage.

2.2 Configuring the ROM/EPROM Array for ROM Size

The MEK68RR Module has eight ROM/EPROM sockets. These are divided into two arrays, which are again subdivided into two clusters of two sockets each. Each cluster must have the same type of ROMs/EPROMs, but one may mix ROMs and EPROMs when using separate clusters. All sockets within an array must be configured for the same size (i.e.: 1K x 8, 2K x 8, 4K x 8, or 8K x 8). Arrays Ø and 1 are configured in the same manner, and the same tables may be used for both. To configure the MEK68RR for ROM/EPROM size, use the jumper locations in Table 2. Note that the MEK68RR, as shipped, is configured for 1K x 8 ROMs/EPROMs.

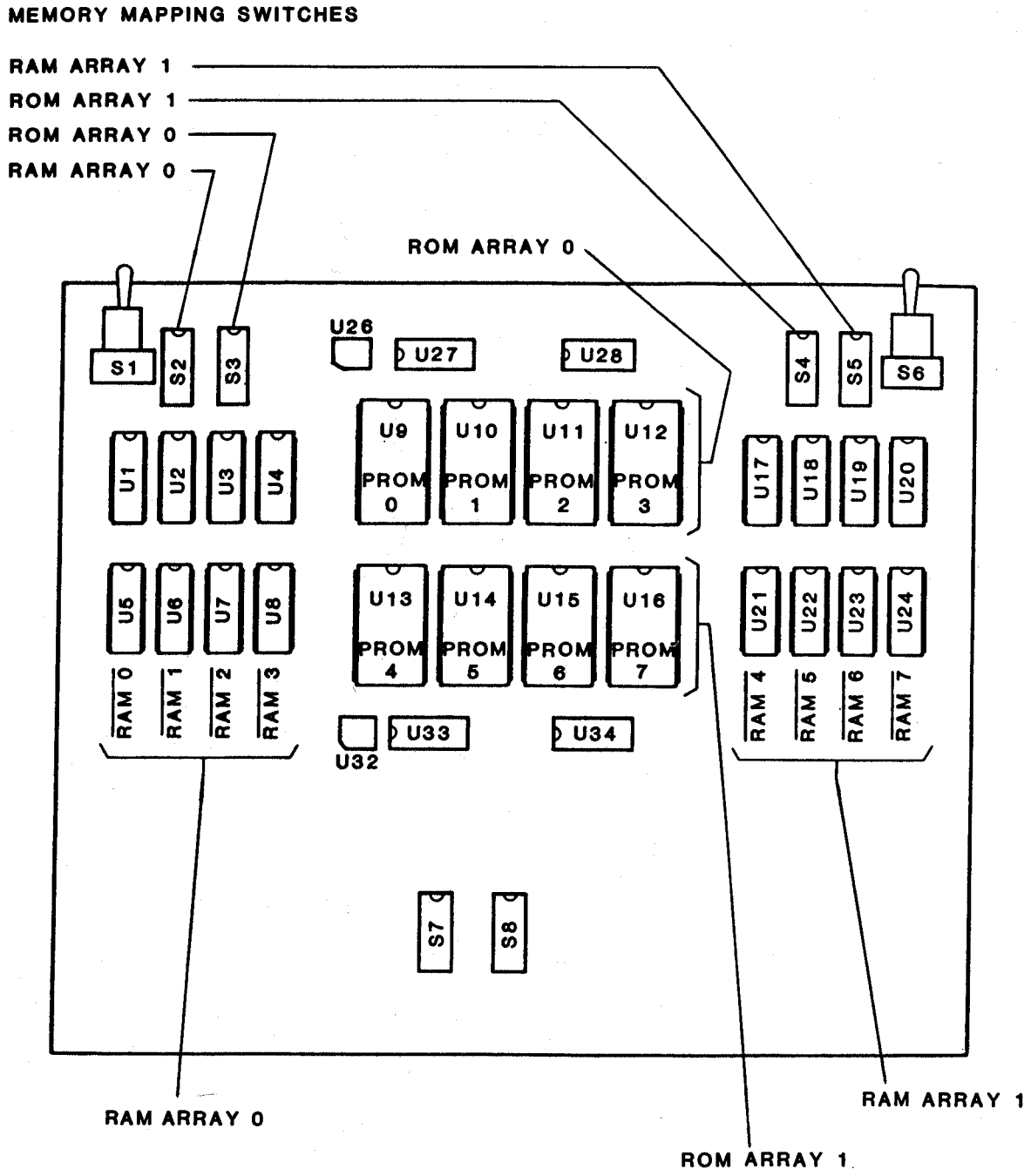


FIGURE 2. MEMORY ARRAY

TABLE 2. CONFIGURING ROM/EPROM SOCKETS FOR ROM SIZE

ROM Array	Jumper Positions	ROM/EPROM Size			
		1K x 8	2K x 8	4K x 8	8K x 8
Ø	U36	3 - 14	4 - 14	5 - 14	6 - 14
		4 - 13	5 - 13	6 - 13	---
		1 - 16	1 - 16	---	---
		2 - 15	---	---	---
	E7	No	No	No	Yes
	E8	Yes	Yes	Yes	No
	E9	Yes	Yes	Yes	No
1	U36	3 - 12	4 - 12	5 - 12	6 - 12
		4 - 11	5 - 11	6 - 11	---
		7 - 10	---	---	---
		8 - 9	8 - 9	---	---
	E5	Yes	Yes	Yes	No
	E6	No	No	No	Yes
	E10	Yes	Yes	Yes	No

2.2 Configuring the ROM/EPROM Array for ROM Size (cont'd)

To change the ROM/EPROM size, the artwork must be cut. Refer to Appendix 5 and cut all paths marked ①→ at the point indicated by an "X".

2.3 Configuring the MEK68RR for ROM/EPROM Type

Each ROM/EPROM socket is individually configurable to accept an assortment of ROMs or EPROMs from 1K x 8 through 8K x 8. However, each ROM within an array must be equal in size. Tables 5 through 12 (located at the end of this chapter) show jumper positioning for the most common types of ROMs/ EPROMs. Array Ø is configured in a similar way to Array 1, and the same table may be used for either. Jumper locations for Array Ø are given without parentheses, and jumper locations for Array 1 are shown in parentheses. Note that at least one of the chip select inputs of each ROM/EPROM must be active low.

The MEK68RR is shipped configured for the MCM2708 EPROM. To re-configure the ROM Arrays to another type, refer to Appendix 5 and cut all traces marked ②→ at the position marked "X".

2.4 Memory Mapping the ROM/EPROM Arrays

Each ROM/EPROM array has a hex rotary switch (S3 for Array Ø and S4 for Array 1). The base address for the entire array is defined by the memory mapping switch, and the base address is indicated by an arrow on the switch armature pointing to a hex digit on the switch dial. All sixteen positions may be used when 1K x 8 ROMs/EPROMs are installed in the array. When 2K x 8 ROMs/EPROMs are used, the total memory space for an array is 8K and only the even base addresses may be used (0XXX, 2XXX, 4XXX, etc.)

TABLE 3. ROM ADDRESS. (SWITCH AND ROM NUMBERS ARE SHOWN FOR ARRAY Ø WITHOUT PARENTHESES, AND FOR ARRAY 1 WITH PARENTHESES).

S3 (S4) Switch Position	PROM 0 (PROM 4)				PROM 1 (PROM 5)				PROM 2 (PROM 6)				PROM 3 (PROM 7)			
	Configured For				Configured For				Configured For				Configured For			
	1Kx8	2Kx8	4Kx8	8Kx8	1Kx8	2Kx8	4Kx8	8Kx8	1Kx8	2Kx8	4Kx8	8Kx8	1Kx8	2Kx8	4Kx8	8Kx8
0	0000	0000	0000	0000	0400	0800	1000	2000	0800	1000	2000	4000	0C00	1800	3000	6000
1	1000	----	----	----	1400	----	----	----	1800	----	----	----	1C00	----	----	----
2	2000	2000	----	----	2400	2800	----	----	2800	3000	----	----	2C00	3800	----	----
3	3000	----	----	----	3400	----	----	----	3800	----	----	----	3C00	----	----	----
4	4000	4000	4000	----	4400	4800	5000	----	4800	5000	6000	----	4C00	5800	7000	----
5	5000	----	----	----	5400	----	----	----	5800	----	----	----	5C00	----	----	----
6	6000	6000	----	----	6400	6800	----	----	6800	7000	----	----	6C00	7800	----	----
7	7000	----	----	----	7400	----	----	----	7800	----	----	----	7C00	----	----	----
8	8000	8000	8000	8000	8400	8800	9000	A000	8800	9000	A000	C000	8C00	9800	B000	E000
9	9000	----	----	----	9400	----	----	----	9800	----	----	----	9C00	----	----	----
A	A000	A000	----	----	A400	A800	----	----	A800	B000	----	----	AC00	B800	----	----
B	B000	----	----	----	B400	----	----	----	B800	----	----	----	BC00	----	----	----
C	C000	C000	C000	----	C400	C800	D000	----	C800	D000	E000	----	CC00	D800	F000	----
D	D000	----	----	----	D400	----	----	----	D800	----	----	----	DC00	----	----	----
E	E000	E000	----	----	E400	E800	----	----	E800	F000	----	----	EC00	F800	----	----
F	F000	----	----	----	F400	----	----	----	F800	----	----	----	FC00	----	----	----

TABLE 4. RAM ADDRESS

	RAM ARRAY 1 - S2				RAM ARRAY 1 - S5			
S4 OR S5 Position	RAM 0 U1,U5	RAM 1 U2,U6	RAM 2 U3,U7	RAM 3 U4,U8	RAM 4	RAM 5	RAM 6	RAM 7
0	0000	0400	0800	0C00	0000	0400	0800	0C00
1	1000	1400	1800	1C00	1000	1400	1800	1C00
2	2000	2400	2800	2C00	2000	2400	2800	2C00
3	3000	3400	3800	3C00	3000	3400	3800	3C00
4	4000	4400	4800	4C00	4000	4400	4800	4C00
5	5000	5400	5800	5C00	5000	5400	5800	5C00
6	6000	6400	6800	6C00	6000	6400	6800	6C00
7	7000	7400	7800	7C00	7000	7400	7800	7C00
8	8000	8400	8800	8C00	8000	8400	8800	8C00
9	9000	9400	9800	9C00	9000	9400	9800	9C00
A	A000	A400	A800	AC00	A000	A400	A800	AC00
B	B000	B400	B800	BC00	B000	B400	B800	BC00
C	C000	C400	C800	CC00	C000	C400	C800	CC00
D	D000	D400	D800	DC00	D000	D400	D800	DC00
E	E000	E400	E800	EC00	E000	E400	E800	EC00
F	F000	F400	F800	FC00	F000	F400	F800	FC00

2.4 Memory Mapping the ROM/EPROM Arrays (cont'd)

hex digit may be used as a base address. Finally, when 8K x 8 ROMs are used, the total memory space for the array is 32K and it may be located at ØXXX or 8XXX. The user is expected to consult the system memory map in the appendix to insure that no address conflicts occur.

2.5 RAM Expansion

The MEK68RR is shipped with 1K x 8 of RAM (two 2114, 1K x 4 chips) on board. There are two RAM arrays partitioned into 4K byte blocks. RAM chips may be added to the board up to a maximum of 8K bytes. When adding RAM, the chips should be inserted into the least significant address space available in the desired array. This will provide for contiguous RAM (see Figure 2, Memory Array).

2.6 Memory Mapping the RAM Arrays

Each RAM array has an individual memory mapping switch (S2 for Array Ø, S5 for Array 1). The base address of the entire array is defined by the mapping switch. The most significant nibble of the base address is indicated by a pointer on the armature of the switch pointing to a hex digit on the switch dial. Note that the RAM arrays may be located anywhere in the memory map. The user is expected to consult the system memory map in the appendix to insure that no memory conflicts occur.

2.7 RAM Write Protect Option

Each RAM array has an independent write protect switch associated with it (S1 for RAM Array Ø, and S6 for RAM Array 1). Under normal use, the write protect switches are switched into the RAM position. This allows

2.7 RAM Write Protect Option (cont'd)

the RAM to be written into and read. When it is desired to change the RAM to read only, the write protect switches are positioned to the ROM position.

2.8 Paging

The MOKEP system supports eight pages for RAM and eight pages for ROM. System control of the paging features is via the paging register on the MEK6802D3 module, and its use is described in the D3 manual. The ROM/EPROM and RAM arrays on the MEK68RR module may be individually configured to appear in any of the eight pages. Consult Table 13 to determine where to place the jumpers.

The MEK68RR module is supplied with jumpers in artwork configuring all arrays to appear in page 1. To cause either the ROM/EPROM arrays or the RAM arrays to appear in pages other than page 1, jumper changes and an artwork cut are required. For the RAM arrays, cut the trace marked ③→ at the location marked "X" (see Appendix 5). For the ROM/EPROM arrays, cut the trace marked ④→ at the location marked "X" (see Appendix 5).

As indicated in Table 13, both ROM arrays and both RAM arrays may be located in separate pages. If it is desired to locate both ROM arrays in the same page pattern, a jumper may be installed in U38, pins 4-5. Otherwise, this jumper is to be removed. Likewise, if both RAM arrays are to appear in the same pattern, a jumper must be installed in U38, pins 3-6. Otherwise, this jumper is to be removed.

TABLE 5. CONFIGURING THE MEK68RR FOR THE MCM68A308 ROM

1K x 8 ROM	MCM68A308	Jumper Installed in U27 (U33) to Configure Socket:			Jumper Installed in U28 (U34) to Configure Socket:		
		PROM Ø (PROM 4) Active Low		Active High	PROM 2 (PROM 6) Active Low		Active High
	CS1 (ROM Pin 18)	4-14	or	4-16	4-14	or	4-16
	CS2 (ROM Pin 19)	7-14	or	7-16	7-14	or	7-16
	CS3 (ROM Pin 20)	3-14			3-14		
	CS4 (ROM Pin 21)	2-14	or	2-16	2-14	or	3-16
		PROM 1 (PROM 5) Active Low		Active High	PROM 3 (PROM 7) Active Low		Active High
	CS1 (ROM Pin 18)	5-11	or	5-16	5-11	or	5-16
	CS2 (ROM Pin 19)	8-11	or	8-16	8-11	or	8-16
	CS3 (ROM Pin 20)	6-11			6-11		
	CS4 (ROM Pin 21)	1-11	or	1-16	1-11	or	1-16

E1 through E4 and E11 through E14 are not to be installed.

TABLE 6. CONFIGURING THE MEK68RR FOR THE MCM68A316E ROM

2K x 8 ROM	MCM68A316E	Jumper Installed in U27 (U33) to Configure Socket:			Jumper Installed in U28 (U34) to Configure Socket:		
		PROM Ø (PROM 4) Active Low		Active High	PROM 2 (PROM 6) Active Low		Active High
	CSØ (ROM Pin 18)	14-4	or	16-4	14-4	or	16-4
	CS1 (ROM Pin 20)	14-3			14-3		
	CS2 (ROM Pin 21)	14-2	or	16-2	14-2	or	16-2
		10-7			10-7		
		PROM 1 (PROM 5) Active Low		Active High	PROM 3 (PROM 7) Active Low		Active High
	CSØ (ROM Pin 18)	5-11	or	5-16	5-11	or	5-16
	CS1 (ROM Pin 20)	6-11			6-11		
	CS2 (ROM Pin 21)	1-11	or	1-16	1-11	or	1-16
		8-10			8-10		

E1 through E4 and E11 through E14 are not to be installed.

TABLE 7. CONFIGURING THE MEK68RR FOR THE MCM68A332 ROMs

4K x 8 ROM	MCM68A332	Jumper Installed in U27 (U33) to Configure Socket:			Jumper Installed in U28 (U34) to Configure Socket:		
		PROM Ø (PROM 4) Active Low		Active High	PROM 2 (PROM 6) Active Low		Active High
CS1	(Pin 21)	2-14	or	2-16	2-14	or	2-16
A10	(Pin 19)	7-10			7-10		
A11	(Pin 18)	4-13			4-13		
CS0	(Pin 20)	3-14			3-14		
		PROM 1 (PROM 5) Active Low		Active High	PROM 3 (PROM 7) Active Low		Active High
CS1	(Pin 21)	1-11	or	1-16	1-11	or	1-16
A10	(Pin 19)	8-10			8-10		
A11	(Pin 18)	5-13			5-13		
CS0	(Pin 20)	6-11			6-11		

E1 through E4 and E11 through E14 are not to be installed.

TABLE 8. CONFIGURING THE MEK68RR FOR THE MCM68A364 ROMs

8K x 8 ROM	MCM68A364	Jumper Installed in U27 (U33) to Configure Socket:	Jumper Installed in U28 (U34) to Configure Socket:
		PROM Ø (PROM 4)	PROM 2 (PROM 6)
A11	(Pin 18)	4-13	4-13
A10	(Pin 19)	7-10	7-10
$\overline{CS0}$	(Pin 20)	3-14	3-14
A12	(Pin 21)	2-12	2-12
		PROM 1 (PROM 5)	PROM 3 (PROM 7)
A11	(Pin 18)	5-13	5-13
A10	(Pin 19)	8-10	8-10
$\overline{CS0}$	(Pin 20)	6-11	6-11
A12	(Pin 21)	1-12	1-12
		E1 (E2)	E3 (E4)

TABLE 9. CONFIGURING THE MEK68RR FOR THE MCM2708 EPROM

1K x 8 EPROM	MCM68708 MCM2708 TMS2708 INT2708	Jumper Installed in U27 (U33) to Configure Socket:	Jumper Installed in U28 (U34) to Configure Socket:
		PROM Ø (PROM 4)	PROM 2 (PROM 6)
VBB (Pin 21)		2-15	2-15
$\overline{CS0}$ (Pin 20)		3-14	3-14
VDD (Pin 19)		7-9	7-9
		PROM 1 (PROM 5)	PROM 4 (PROM 7)
VBB (Pin 21)		1-15	1-15
$\overline{CS0}$ (Pin 20)		6-11	6-11
VDD (Pin 19)		8-9	8-9

E1 through E4 and E11 through E14 are not to be installed.

TABLE 10. CONFIGURING THE MEK68RR FOR THE TMS2716 EPROM

2K x 8 EPROM	TMS2716	Jumper Installed in U27 (U33) to Configure Socket:	Jumper Installed in U28 (U34) to Configure Socket:
		PROM Ø (PROM 4)	PROM 2 (PROM 6)
VBB	(Pin 21)	2-15	2-15
A10	(Pin 20)	3-10	3-10
$\overline{S}$/PGR	(Pin 18)	4-14	4-14
VDD	(Pin 19)	7-9	7-9
		PROM 1 (PROM 5)	PROM 3 (PROM 7)
VBB	(Pin 21)	1-15	1-15
$\overline{S}$/PGR	(Pin 18)	5-11	5-11
A10	(Pin 20)	6-10	6-10
VDD	(Pin 19)	8-9	8-9

E3, E4, E12, E13 are not to be installed.

TABLE 11. CONFIGURING THE MEK68RR FOR THE MCM2716 EPROMs

2K x 8 EPROM	MCM2716 TMS2516 INT2716	Jumper Installed in U27 (U33) to Configure Socket:	Jumper Installed in U28 (U34) to Configure Socket:
		PROM Ø (PROM 4)	PROM 2 (PROM 6)
VPP	(Pin 21)	2-16	2-16
$\overline{G}$	(Pin 20)	3-14	3-14
$\overline{E}$/PGR	(Pin 18)	4-12	4-12
A10	(Pin 19)	7-10	7-10
		PROM 1 (PROM 5)	PROM 3 (PROM 7)
VPP	(Pin 21)	1-16	1-16
$\overline{E}$/PGR	(Pin 18)	5-12	5-12
$\overline{G}$	(Pin 20)	6-11	6-11
A10	(Pin 19)	8-10	8-10
		E4 (E12)	E3 (E13)

TABLE 12. CONFIGURING THE MEK68RR FOR THE TMS2532 EPROMs

4K x 8 EPROM	TMS2532	Jumper Installed in U27 (U33) to Configure Socket:	Jumper Installed in U28 (U34) to Configure Socket:
		PROM Ø (PROM 4)	PROM 2 (PROM 6)
+5 V (Pin 21)		2-16	2-16
$\overline{CS0}$ (Pin 20)		3-14	3-14
BA11 (Pin 18)		4-13	4-13
BA10 (Pin 19)		7-10	7-10
		PROM 1 (PROM 5)	PROM 3 (PROM 7)
+5 V (Pin 21)		1-16	1-16
BA11 (Pin 18)		5-13	5-13
$\overline{CS1}$ (Pin 20)		6-11	6-11
BA10 (Pin 19)		8-10	8-10

E1 through E4 and E11 through E14 are not to be installed.

TABLE 13. ROM AND RAM PAGING JUMPER LOCATIONS

Page	ROM Array Ø	ROM Array 1	RAM Array Ø	RAM Array 1
	Jumper Located in S7 from Pins 16,15,14,13 to S7 Pin:	Jumpers Located in S7 from Pins 12,11,10,9 to S7 Pin:	Jumpers Located in S6 from Pins 16,15,14,13 to S8 Pin:	Jumper Located in S8 from Pins 12,11,10,9 to S8 Pin:
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
4	4	4	4	4
5	5	5	5	5
6	6	6	6	6
7	7	7	7	7
8	8	8	8	8

APPENDIX 1

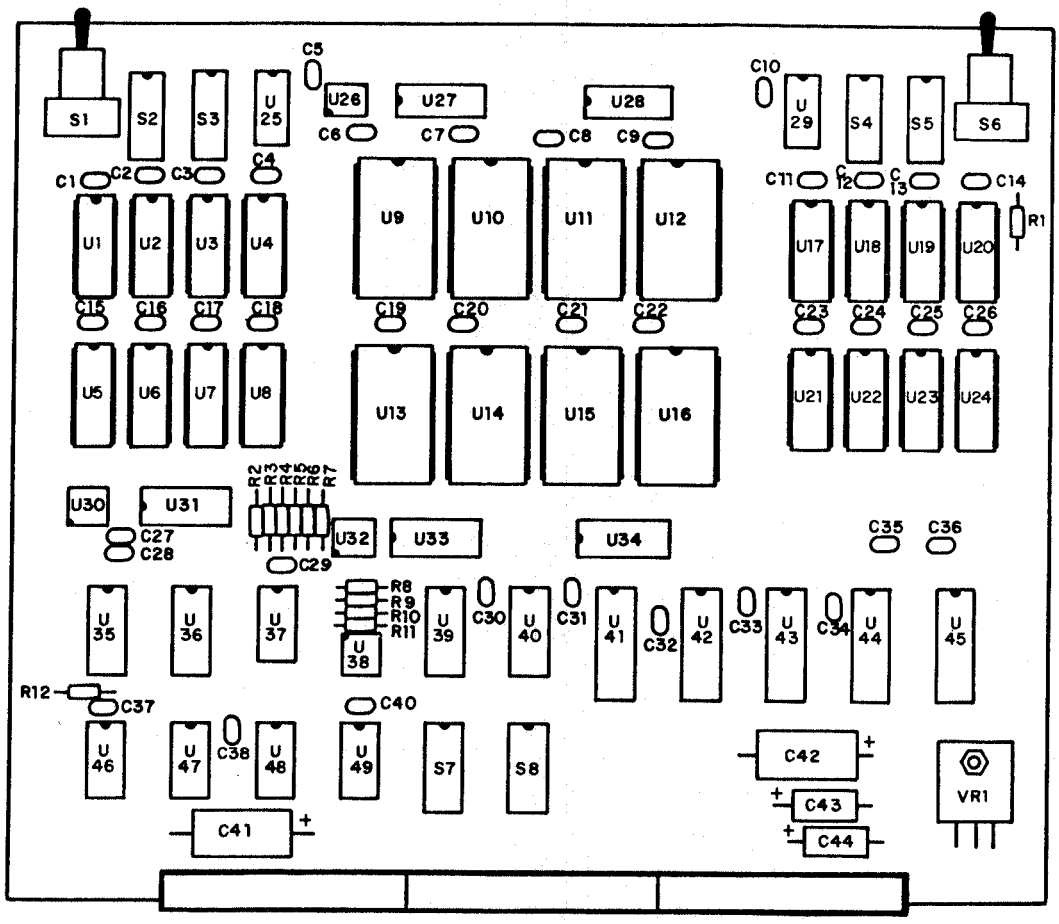
SHIPPING LIST

Item Number	Description
1	MEK68RR PC Board
2	MEK68RR User's Manual

APPENDIX 2

PARTS LAYOUT

APPENDIX 2. PARTS LAYOUT



APPENDIX 3

BUS PINOUT AND DESCRIPTION

APPENDIX 3. BUS PINOUT AND DESCRIPTION

Pin Number	Signal Mnemonic	Signal and Description
1	GND	Ground
2	E	Enable - System Ø2 clock.
3	---	N.C.
4	+5 V	+5 V Power Supply.
6	---	N.C.
7	---	N.C.
8	---	N.C.
9	VMA	Valid Memory Address - A logic zero of this pin indicates invalid bus memory address or data.
10	---	N.C.
11	R/$\overline{W}$	Read/Write - This signal indicates the direction of data flow on the Data Bus. A "1" indicates data flowing from the bus to the processor card and "Ø" indicates data flowing from the processor card to the bus.
12	GND	Ground
13	$\overline{RESET}$	Reset - When this line is held low, the processor is held in the reset mode.
14	---	N.C.
15	---	N.C.
16	---	N.C.
17	---	N.C.
18	---	N.C.
19	GND	Ground
20	KEY SLOT	
21	ROPØ	ROM PAGE Ø - LSB of 3 line encoded ROM page signal.

APPENDIX 3. BUS PINOUT AND DESCRIPTION (cont'd)

Pin Number	Signal Mnemonic	Signal and Description
22	ROP1	ROM Page 1 - ROM page signal line 1.
23	ROP2	ROM page 2 - ROM page signal line 2.
24	RAPØ	RAM page Ø - LSB of 3 line encoded RAM page signal.
25	RAP1	RAM page 1 - RAM page signal line 1.
26	RAP2	RAM page 2 - RAM page signal line 2.
27	----	N.C.
28	----	N.C.
29	----	N.C.
30	AØ	Address Bus Ø - Transfers address information from the processor card to other cards on the bus.
31	A1	Address Bus 1 - Transfers address information from the processor card to other cards on the bus.
32	A2	Address Bus 2 - Transfers address information from the processor card to other cards on the bus.
33	A3	Address Bus 3 - Transfers address information from the processor card to other cards on the bus.
34	A4	Address Bus 4 - Transfers address information from the processor card to other cards on the bus.
35	A5	Address Bus 5 - Transfers address information from the processor card to other cards on the bus.
36	A6	Address Bus 6 - Transfers address information from the processor card to other cards on the bus.
37	A7	Address Bus 7 - Transfers address information from the processor card to other cards on the bus.
38	A8	Address Bus 8 - Transfers address information from the processor card to other cards on the bus.
39	A9	Address Bus 9 - Transfers address information from the processor card to other cards on the bus.

Pin Number	Signal Mnemonic	Signal and Description
40	A10	Address Bus 10 - Transfers address information from the processor card to other cards on the bus.
41	A11	Address Bus 11 - Transfers address information from the processor card to other cards on the bus.
42	A12	Address Bus 12 - Transfers address information from the processor card to other cards on the bus.
43	A13	Address Bus 13 - Transfers address information from the processor card to other cards on the bus.
44	A14	Address Bus 14 - Transfers address information from the processor card to other cards on the bus.
45	A14	Address Bus 15 - Transfers address information from the processor card to other cards on the bus.
46	GND	Ground
47	GND	Ground
48	DØ	Data Bus Ø - This bidirectional line, when enabled, provides 2 way data transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
49	D1	Data Bus 1 - This bidirectional line, when enabled, provides 2 way data transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
50	D2	Data Bus 2 - This bidirectional line, when enabled, provides 2 way data transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
51	D3	Data Bus 3 - This bidirectional line, when enabled, provides 2 way data transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
52	D4	Data Bus 4 - This bidirectional line, when enabled, provides 2 way data transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.

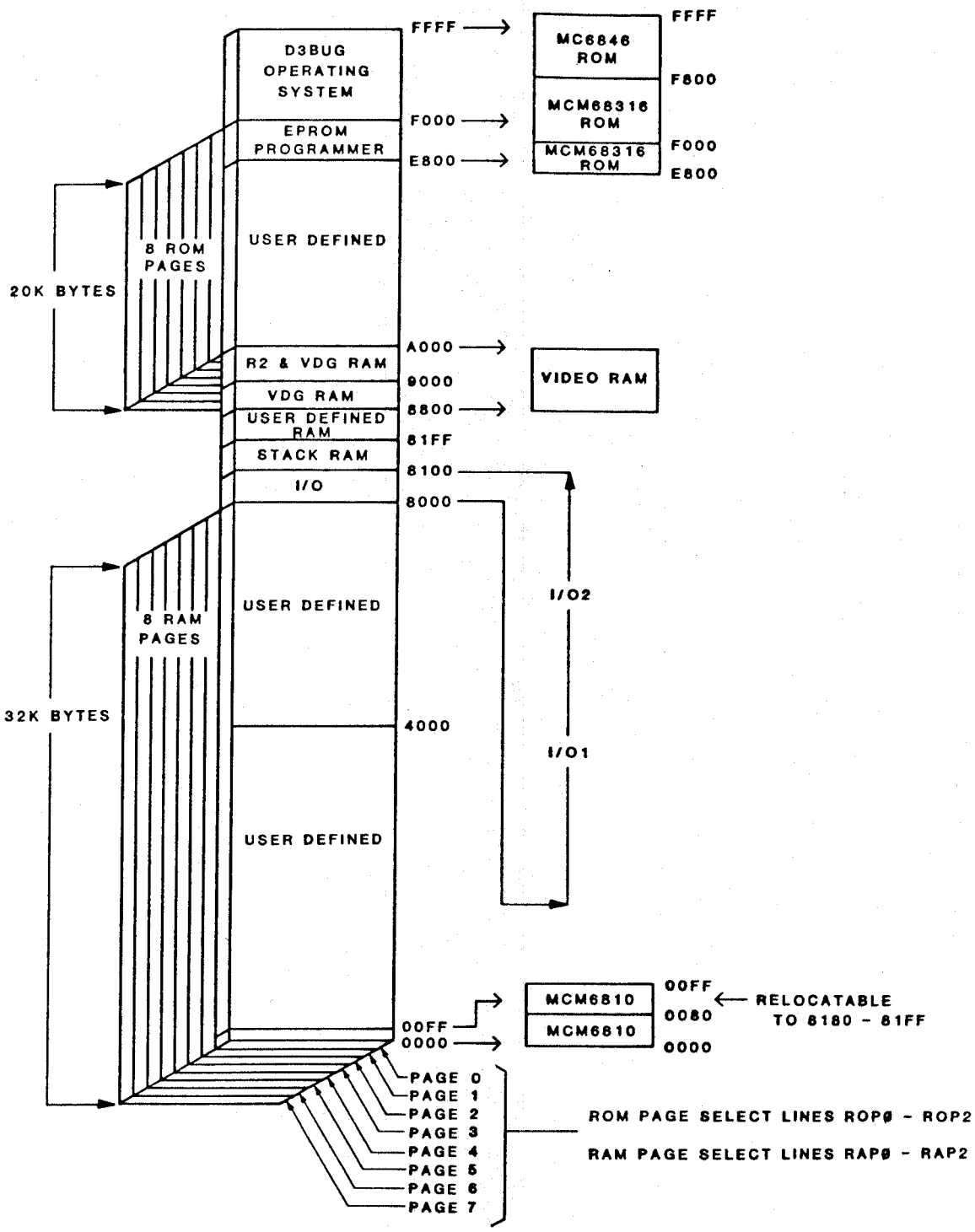
APPENDIX 3. BUS PINOUT AND DESCRIPTION (cont'd)

Pin Number	Signal Mnemonic	Signal and Description
53	D5	Data Bus 5 - This bidirectional line, when enabled, provides 2 way transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
54	D6	Data Bus 6 - This bidirectional line, when enabled, provides 2 way transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
55	D7	Data Bus 7 - This bidrectional line, when enabled, provides 2 way transfer between the processor card and other cards in the system. The direction is determined by R/$\overline{W}$.
56	+12 V	+12 V Power Supply.
57	GND	Ground
58	-12 V	-12 V Power Supply.
59	+5 V	+5 V Power Supply.
60	GND	Ground

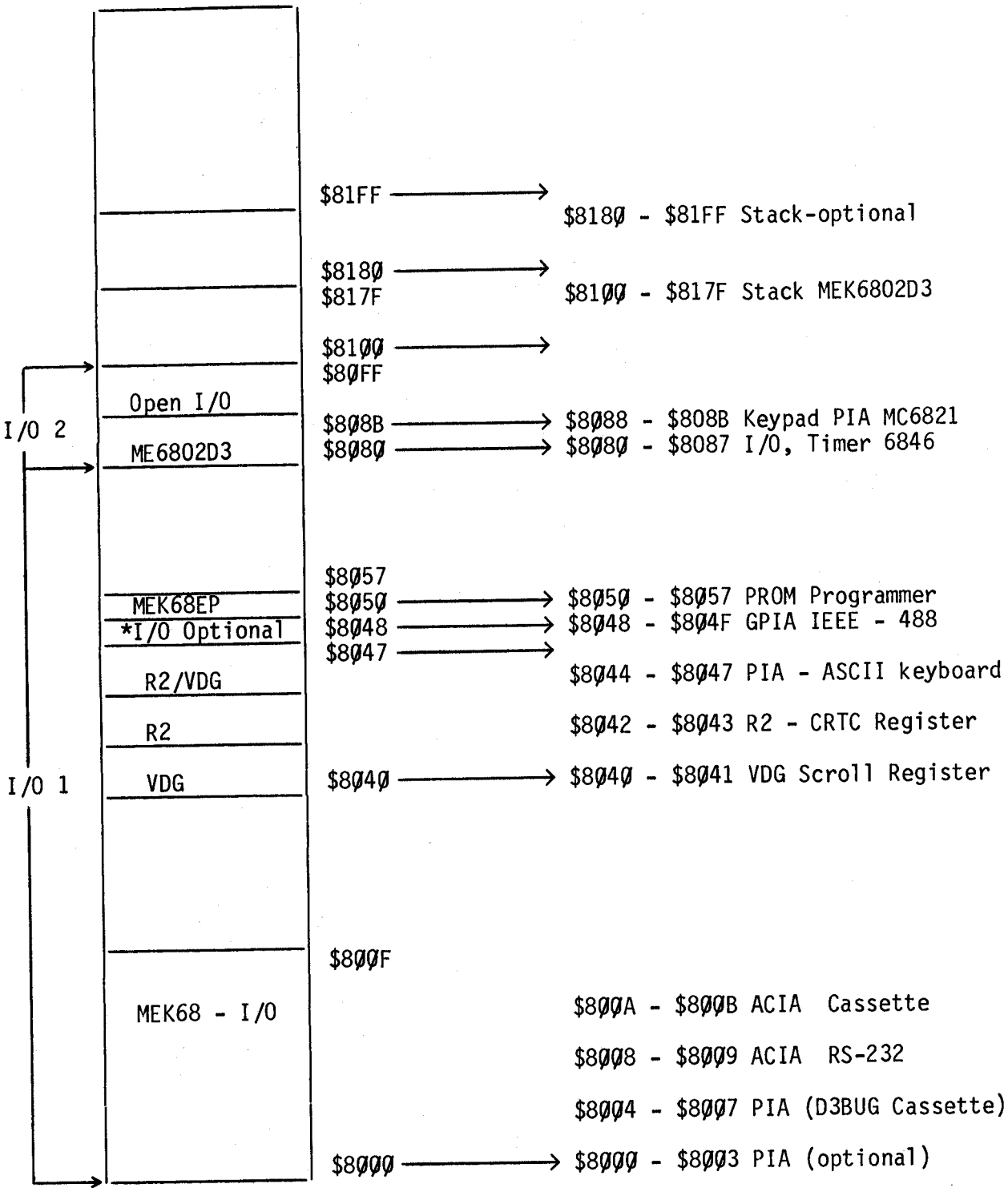
APPENDIX 4

MOKEP MEMORY MAP

APPENDIX 4. MEMORY MAP



APPENDIX 4. MEMORY MAP (cont'd)

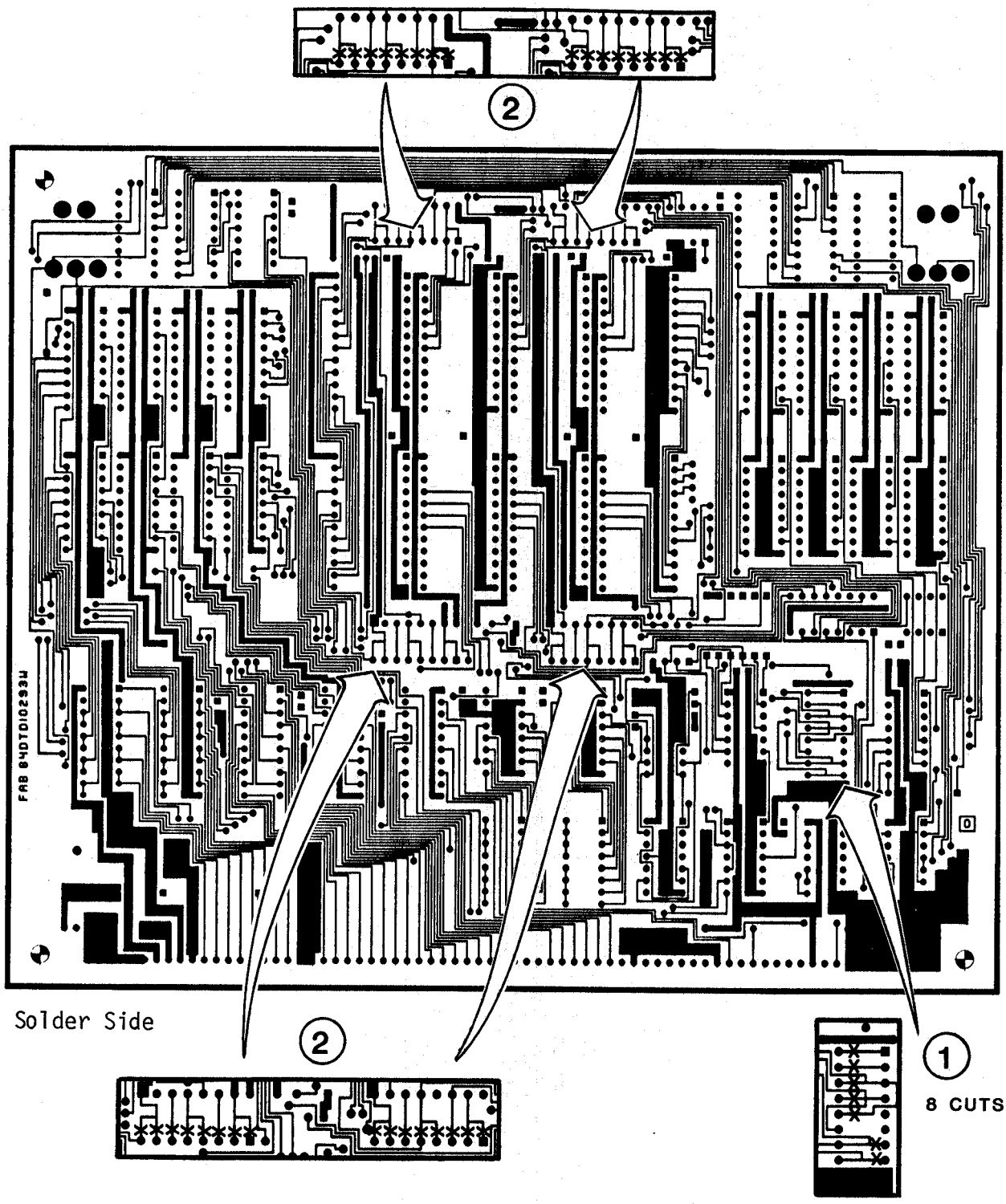


*See MEK68IO manual for details.

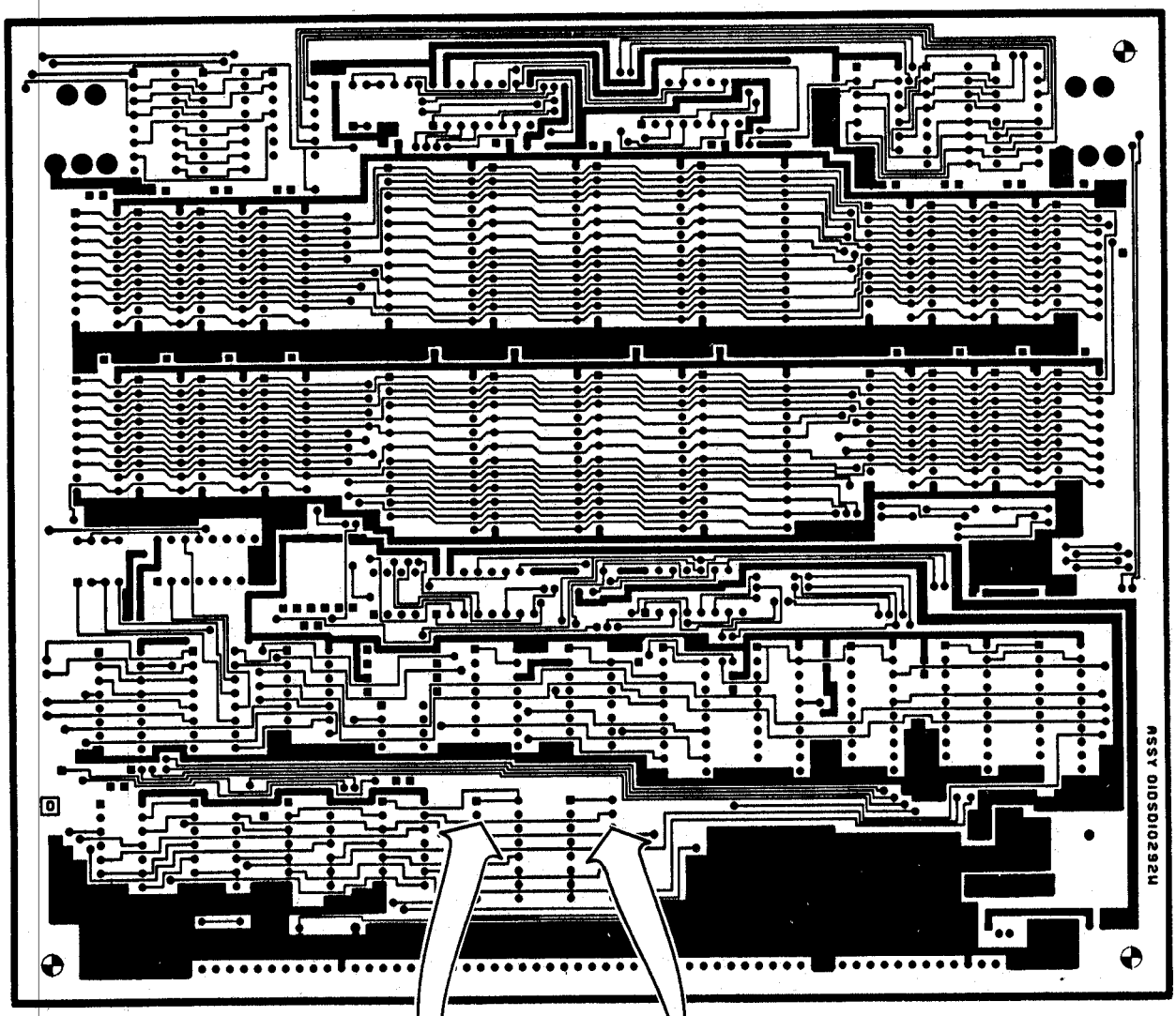
APPENDIX 5

ARTWORK CUTTING DIAGRAM

APPENDIX 5. ARTWORK CUTTING DIAGRAM



APPENDIX 5. ARTWORK CUTTING DIAGRAM (cont'd)



Component Side

APPENDIX 6

PARTS LIST

APPENDIX 6. PARTS LIST

Item Number	Quantity	Description	Part Number	Reference Designation
1	1	PC Board	MEK68RR	
2	1	Integrated Circuit	74LS00	U48
3	2	Integrated Circuit	74LS04	U29,U49
4	1	Integrated Circuit	74LS10	U46
5	2	Integrated Circuit	74LS21	U37, U25
6	2	Integrated Circuit	74LS139	U31, U35
7	2	Integrated Circuit	74LS156	U39, U40
8	5	Integrated Circuit	74SL244	U41-U45
9	1	Integrated Circuit	74LS20	U47
10	2	Integrated Circuit	MCM2114P45	U1, U5
11	4	Switch, Hex Rotary	*	S2 - S5
12	39	Capacitor, 0.1 Micro Farad Monolithic Ceramic		C1-C38, C40
13	1	Capacitor, 1.0 Micro Farad Aluminum Electrolytics		C44
14	1	Capacitor, 2.2 Micro Farad Aluminum Electrolytics		C43
15	2	Capacitor, 100 Micro Farad		C41, C42
16	12	Resistor, 10K ohm 1/4 Watt, 5%		R1 - R12
17	2	Socket, IC, 8 Pin		U26,U30,U32, U38
18	11	Socket, IC, 16 Pin		S2-S5,S7,S8, U27,U28,U33, U34,U36
19	16	Socket, IC, 18 Pin		U1-U8,U17-U24

APPENDIX 6. PARTS LIST (cont'd)

Item Number	Quantity	Description	Part Number	Reference Designation
20	8	Socket, IC, 24 Pin		U9 - U16
21	1	Voltage Regulator MC7905 CT/CP		VR1
22	2	Switch, Toggle	**	S1, S6
23	3	Connector, R/A 20	***	P1
24	1	Key, Polar	***	(For P1)
25	10	Jumper Pin		(Ref U26,U30, U32,U38)
26	1	Screw, 4-40 x 1/4 PPH		(Ref Only)
27	1	Nut, 4-40 Hex		(Ref Only)

* Amy Inc.
Harrisburg, Pa. 17105

** Cutler-Hammer
Specialty Products Div.
Milwaukee, Wisc. 53201

*** Molex Inc.
2222 Wellington Ct.
Lisle, Ill. 60532

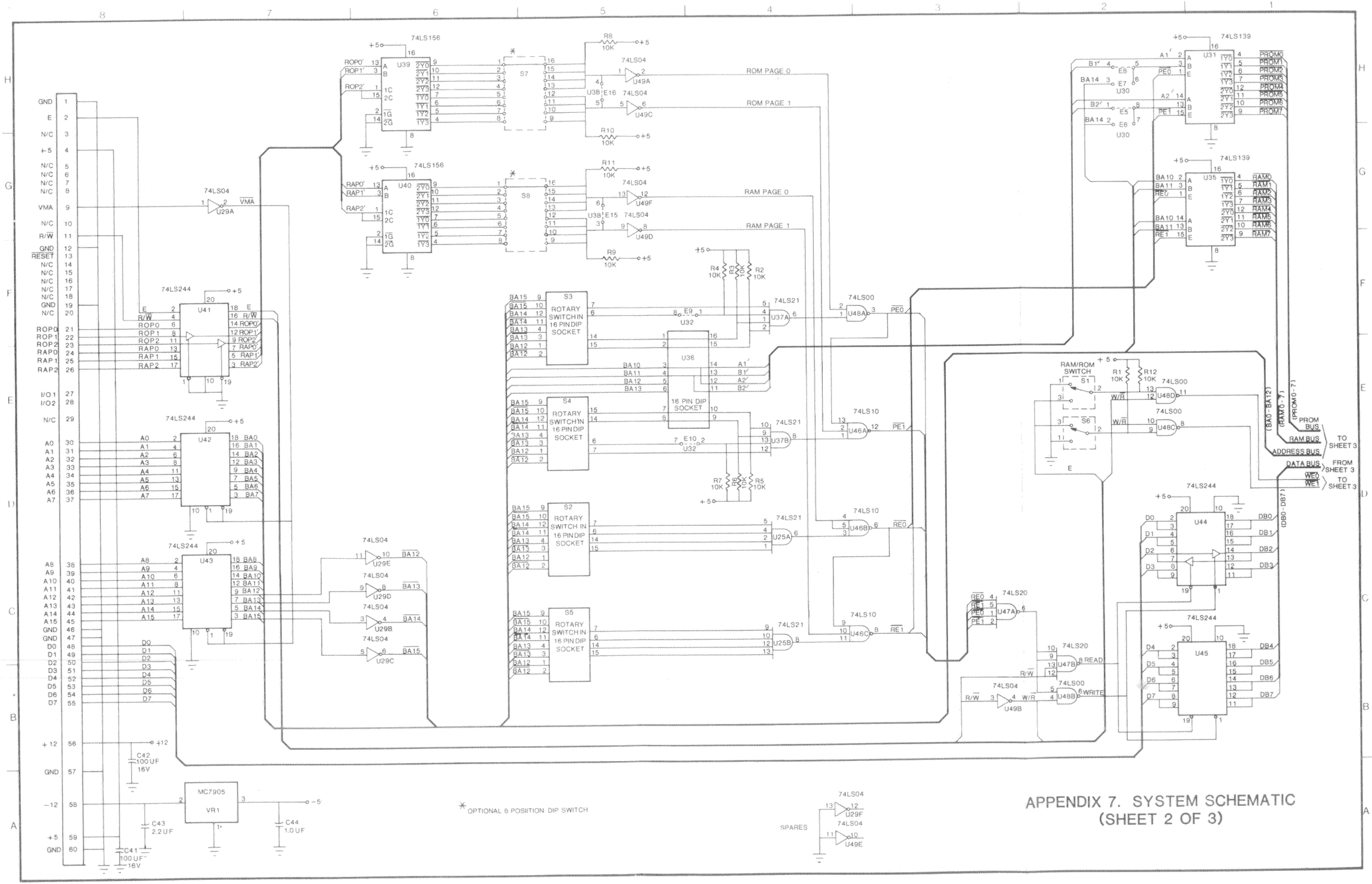
APPENDIX 7

SYSTEM SCHEMATIC

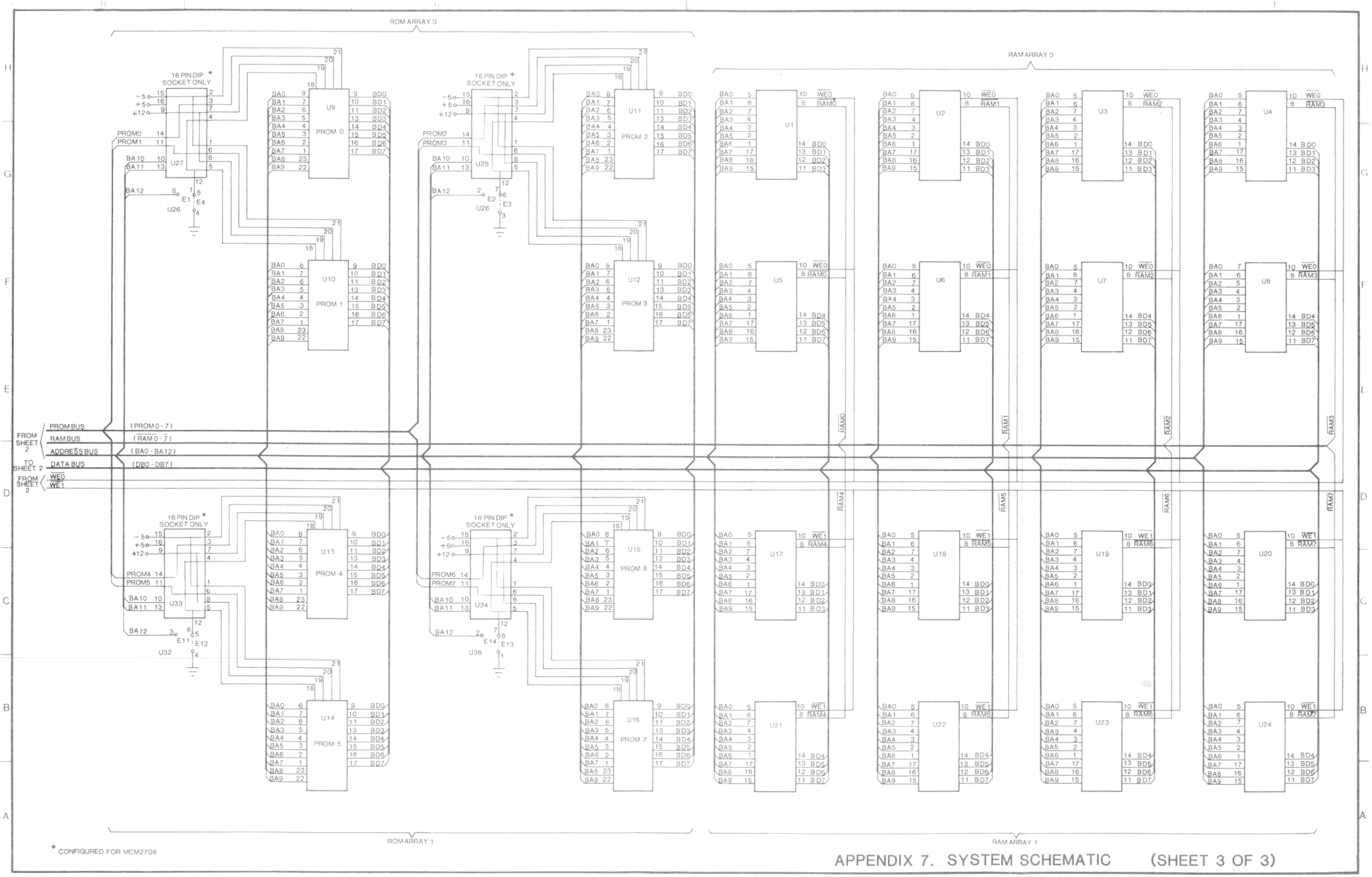
Sheet 1: Index Page

Sheet 2: System Schematic

Sheet 3: System Schematic



APPENDIX 7. SYSTEM SCHEMATIC (SHEET 2 OF 3)



APPENDIX 7. SYSTEM SCHEMATIC (SHEET 3 OF 3)