The 6809 Microsystem - Specifications

Physical

The 6809 Microsystem is based on the 114,3mm x 201mm (4,5" x 8") Verocard which features a 42-way keyed edge connector. Power supplies of +5V, -5V, +12V and -12V are present on the bus.

System Description

Six cards are available at present for the 6809 Microsystem. These are:

1) The 6809 processor card.
2) The 64K dynamic RAM card.
3) The dual serial (RS232) interface card.
4) The 80-line parallel interface card.
5) The memory-mapped VDU card.
6) The floppy disc controller card.

Various versions of the Microsystem may be constructed using some or all of these cards.

THE BASIC SYSTEM consists of the 6809 CPU card, the 64K RAM card and the serial I/O card. This allows communication with the system via a Teletype or other terminal device, and with the addition of other parallel interface cards forms an ultra-powerful controller system for dedicated applications.

THE SIMPLE HOME COMPUTER consists of the 6809 CPU card, the RAM card, parallel I/O card and memory-mapped VDU card. This permits a readily available keyboard and the users domestic TV set to be used for I/O and is the recommended starting system. This system allows the full use of medium resolution graphics via the VDU's programmable character generator, and forms the basis of more powerful versions of the Microsystem.

THE ADVANCED HOME COMPUTER is created by the addition of the floppy disk controller card to the simple home computer. This allows up to four 5,25" minifloppy disc drives to be attached to the system. The user now has the capability to run disk operating systems such as FLEX (from Technical Systems Consultants) which in turn opens the way to advanced editors, assemblers and high-level languages like Pascal, BASIC, FORTH and others. Extra peripheral devices such as printers may be easily added to the system by means of extra parallel and serial cards if necessary.

THE SUPER COMPUTER! Hardware modifications to the advanced home computer permit the system memory capacity to be increased to 256K bytes. The memory chips used on the RAM card must be replaced by the higher density versions, but otherwise no extra expense is involved and the modifications can be made in one evening. At this level the memory management capabilities of the CPU card (which are available at ALL levels of the 6809 Microsystem) are used to their fullest extent. With the addition of (existing) software, the Super-Computer becomes a multi-user system capable of running a number of programs simultaneously.

The Super-Computer far exceeds the capabilities of any other common home computer and is unique in that it may be achieved via a series of expansions through systems that at each stage form powerful computers in their class.

The 6809 Microsystem at any level forms a computer system that is on the one hand a self-contained unit suitable for the software enthusiast while at the same time providing full facilities for the hardware enthusiast who may wish to experiment with computer interfacing and control. As such it is the ideal system for almost any person who is interested in, and involved with, microcomputers.

History

The origins of the 6809 Microsystem go back to the beginning of the Cape Computer Club, when a small group of like-minded people formed a sub-group of the Club devoted to the Motorola microprocessor family, which at that time consisted of the 6800 and 6802 processors. The decision was made to design and build a complete home computer system, modularity and flexibility being assured by the use of a number of separate cards linked by a common bus structure. The decision of what card size and bus to use was answered when the Club introduced the Cape Computer Club bus standard or C3Bus (which defined the card size). A number of initial versions of the Microsystem appeared, based on the C3Bus, but poor support of the bus by the majority of Club members forced the Club to reverse its earlier decision and to adopt instead the newly-appeared SABus national bus standard as its standard.

Investment by the 6800 Group in the C3Bus at this stage made it impossible for us to follow the Club to the SABus, but we were now able to make changes to the C3Bus to make it more suitable for the 6800 family of processors. Around this time the 6809 processor was finally released by Motorola, and the decision was made by the group to design a powerful system around it.

After an initial period of design and discussion, an energetic development phase began in late 1981 with the design and successful production of a high-capacity memory card, 6809 processor card, parallel interface card, floppy disk controller card, memory-mapped video display card and serial interface card - all achieved within the space of approximately eleven months.

Although the design goals for 1981/2 have now been attained, the 6809 Microsystem will not become dormant. Additions to the VDU card in the form of high-resolution graphics boards are already in the design stage, and new additions to the range of peripherals - such as hard discs - are waiting only for the prices to drop to levels affordable by the home computer user. In this way the 6809 Microsystem will always be expanding to remain with the current level of technology.

C3BUS PIN DESCRIPTIONS

1	+5V	Power
2	-5V	Power
3	+12V	Power
4	-12V	Power
5	RESET	Active low, resets all cards on bus
6	E (CLK)	1MHz square wave clock, data transfers during high period
7	--------	KEY
8	A0	Least significant address bit
9	A1	.
10	A2	.
11	A3	.
12	A4	.
13	A5	.
14	A6	.
15	A7	.
16	A8	.
17	A9	.
18	A10	.
19	A11	.
20	A12	.
21	A13	.
22	A14	.
23	A15	Most significant address bit for 64K system
24	WAIT	Active low, to extend memory accesses (E high period)
25	D0	Least significant data bit
26	D1	.
27	D2	.
28	D3	.
29	D4	.
30	D5	.
31	D6	.
32	D7	Most significant data bit
33	HALT	Active low to halt the processor
34	BA	Low indicates CPU halted and busses tristate
35	VMA/A17	Active high Valid Memory Address, MS address bit on 256K system
36	NMI	Active low Non-Maskable Interrupt to CPU
37	IRQ	Active low maskable Interrupt Request to CPU
38	RDS	Active low Read Data Strobe, synchronised with E
39	WDS	Active low Write Data Strobe, synchronised with E
40	IOS/A16	Active low I/O Select, second MS address bit on 256K system
41	R/W	Read/Write, high for read cycle, low for write cycle
42	GND	Supply Ground
43	GND	Supply Ground

C3BUS 6809 CPU CARD

Jonathan Eva

Introduction

The C3Bus 6809 CPU card is designed to allow the use of the Motorola 6809 processor on the C3Bus. It is intended that the card, together with RAM and I/O of some type, will form the nucleus of an advanced and powerful computing system. To this end, several features are included on the card:

i) On-board EPROM (2716 or 2732) allows the system monitor to reside on the CPU card, obviating the need for a separate EPROM card.

ii) Dynamic Address Translation on card allows the expansion of the address bus to up to eighteen bits and thus increases the addressing capability to 256K bytes if required.

iii) Variable I/O addressing allows the selection of a 256-byte page of I/O addresses if required.

Description of Operation

The operation of 6809 CPU will not be described in detail here. The 6809 data sheet should be consulted for these details.

A 1MHz CPU is used, so a 4MHz crystal is required. The power-on reset pulse is generated by U11, a 555 timer. An inverter (U10) in conjunction with a Ge diode converts this signal to an open-collector low-going pulse. The 555 may be triggered by a switch connected across the terminal points provided. The RESET bus line may be subsequently grounded to reset the CPU.

WAIT and HALT bus lines go straight to the 6809 - in the case of the HALT line, a D flip-flop is used to ensure that the HALT transition does not occur at any undesirable time.

Interrupts NMI and IRQ are also fed to the CPU. IRQ may be connected via DIL switches to either IRQ or FIRQ on the CPU to allow the use of fast interrupt servicing when desired.

CPU lines E (Enable), BA (Bus Available) and R/W (Read/ Write) are buffered onto the bus. R/W is tristated during a halted state to allow other master devices use of this line.

The I/O page selection logic is formed by U5 and U6 and selects one of six possible addresses for the I/O page: 90xx, A0xx, B0xx, C0xx, D0xx or E0xx. These addresses are selected after translation has occurred and thus correspond to physical bus Kocations. The six outputs are fed via DIL switches to the IOS bus line.

The address bus A0-A15 and control lines R/W, IOS, VMA, MEMRD

and MEMWR are buffered by U13, 14 and 15 and are tristated during BA (halted state). These five control signals have pullup resistors provided to prevent spurious signals during a HALT.

The data bus is buffered by U16, an LS245, enabled only during the E high period. U19 controls the enable and direction lines of U16 to allow other master devices to access the on-board EPROM U17 while the 6809 is halted. In normal operation, U16 is disabled while U17 is being addressed. U18 provides decoding for a read from the top 2K or 4K of memory to yield the Chip Select signal for U17. Bus line A11 is switched either to U17 or U18 via DIL switches to allow the use of 2716 or 2732 type EPROMs.

U2, U3 and U4, together with extra decoding by U7, U8 and U9 perform the address translation function. U3 and U4 form a 16x6 bit RAM with the four most significant address bits A15-A12 normally connected to the address inputs. The six outputs of the RAM form the most significant six bits of the eighteen bit address bus. We refer to the sixteen bit address from the CPU as a "logical" address, and the eighteen bit address formed by translation by the RAM as a "physical" address, since it corresponds to the actual address appearing on the bus. Consequently, we may make any one of sixty-four physical addresses appear on the bus in response to one logical address from the CPU by simply changing the contents of the appropriate RAM location.

U7, U8 and U9 detect a write or read to the top 256 memory locations and disable the DAT RAM at this time. The outputs of the RAM are forced high, and this ensures a safe power-on reset since the RAM contents will be undefined at this stage. By disabling the RAM, physical addresses 3FFxx are forced to correspond to logical addresses FFxx so the top 256 bytes of the monitor may be successfully executed. A write to these locations causes the multiplexer U2 to switch over, connecting the lower four bits of the address bus to the RAM address inputs. This allows data to be successfully written to the RAM. Note that the sixteen RAM locations fold back through the top 256-byte page.

The two most significant outputs of the RAM are fed via DIL switches to the IOS and VMA bus lines. If a sixteen bit address bus is desired, these top two address lines may be left disconnected, in which case VMA will be tied high and IOS may be fed from U5 as described previously. This means that a sixteen-bit logical bus is being translated to a sixteen-bit physical bus, which allows one to arrange the physical devices attached to the bus in any order in the logical address map - for example, one may arrange RAM which is widely scattered physically into an orderly contiguous block, or vice versa.

Assembly

Assembly of the board is not difficult. Reference should be made to the component overlay provided. Should any doubt exist as to the position of any of the discrete components, the overlay has been drawn to scale and can be used to accurately

identify the correct holes.

Switching Details

Four sets of DIL switches are provided on the board. Their position is marked on the component overlay.

DIL switches A: Used to select whether IRQ or FIRQ on the CPU is connected to bus line IRQ (INTR).

Switch 4 on, 2 off - selects IRQ
Switch 2 on, 4 off - selects FIRQ

Switches 1 and 3 not used.

DIL switches B: Used to select whether a 2716 or 2732 is used as the on-board EPROM. The EPROM will reside in the top 2K or 4K as appropriate.

Switch 1&3 on, 2&4 off - 2716
Switch 2&4 on, 1&3 off - 2732

DIL switches C: Used to select an eighteen or sixteen bit address bus. Also used to select the address of the I/O page.

For an 18-bit bus:
Switch 1&2 on, 3-8 off.

For a 16-bit bus:
Switch 1&2 off, and ONE of 3-8 on according to this table:

Switch 3 on for I/O at 9000-90FF
" 4 " " " " A000-A0FF
" 5 " " " " B000-B0FF
" 6 " " " " C000-C0FF
" 7 " " " " D000-D0FF
" 8 " " " " E000-E0FF

NOTE: For 680X Group members, the correct switch positions for the supplied monitor are:
A: 1-3 off, 4 on
B: 1&3 off, 2&4 on
C: 1-7 off, 8 on

For the fully-expanded 256K system, the correct settings are:
A: 1-3 off, 4 on
B: 1&3 off, 2&4 on
C: 3-8 off, 1&2 on

COMPONENTS LIST

Integrated Circuits

1	6809	1MHz CPU
3	74LS244	Octal Buffers
2	74LS30	NAND Gates
1	74LS32	OR Gates
1	74LS138	3-8 Decoder
2	74LS189	16x4 RAM *see later*
1	74LS02	NOR Gates
1	74LS00	NAND Gates
1	74LS86	EXOR Gates
1	74LS04	Inverters
1	74LS157	2-i/p Multiplexers
1	74LS245	Buffers
1	74LS74	D Flip-flops
1	555	Timer

1 2716/2732 monitor EPROM

Resistors

20	3k3	1/4W
1	10k	"
1	82k	"

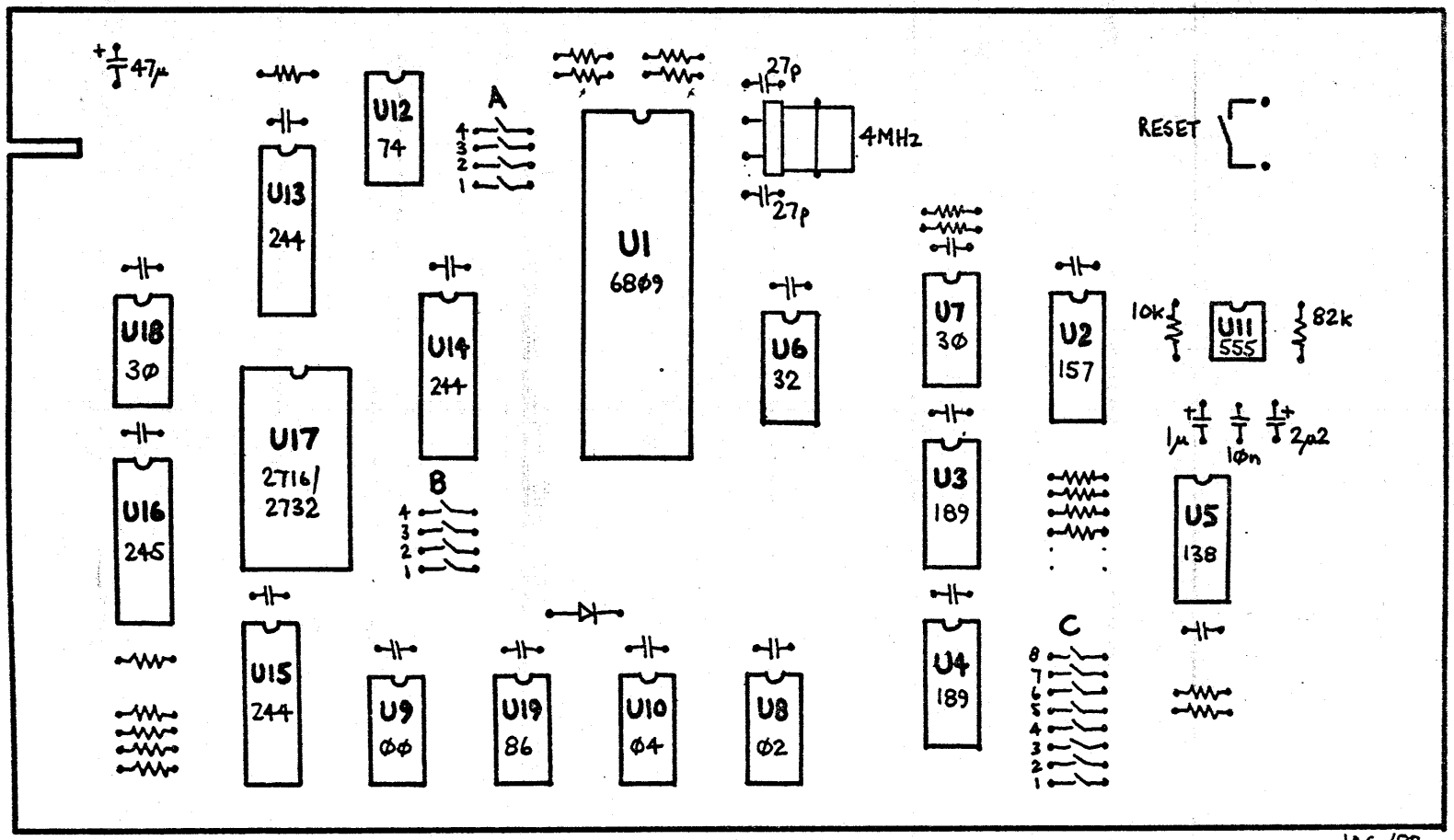
Capacitors

15	100n	Ceramic
2	27p	"
1	47u	Tantalum
1	1u	"
1	2u2	"
1	10n	"

Miscellaneous

2 4-way DIL switches
1 8-way " "
1 4MHz crystal
1 OA91, AAZ15 etc. Ge diode

NOTE: The RAM chips (74LS189) may be replaced by any pin-compatible 16x4 TTL RAMs. Either open collector or tri-state output types may be used. Some alternatives are 7489, 74LS89, 74S89, 74189, 74S189, 74289, 74LS289, 3101, 4103.



COMPONENT OVERLAY

NOTE: ALL UNMARKED CAPACITORS 100nF
ALL UNMARKED RESISTORS 3k3

C3BUS 64K/256K DYNAMIC RAM BOARD

Jonathan Eva

Introduction

This board was designed to allow memory expansion on computers based on the 6800, 6802 or 6809 processors running on the C3Bus. Memory may be added in 16K blocks up to a maximum of 64K. The readily available 4116 16K x 1 dynamic RAM chips are used, and refresh is totally transparent to the user - no wait cycles or clock stretching is employed. The board may be relatively easily expanded using 64K x 1 chips and some modifications to the PC board. No additional circuitry is required.

Note that where the documentation differs for the fully-expanded 256K board, the appropriate values or words for the 256K case are placed in parentheses.

The Dynamic RAM Controller

In this circuit, the recently released Advanced Micro Devices Am2964B RAM controller is used. This device incorporates an Address Multiplexer, Refresh Counter, Row Address Strobe selector and Column Address Strobe buffer in a 40-pin package. Schottky technology is used for very high speed and all address paths are 8 bits wide for use with 64K RAM chips. Timing is external to the device.

A block diagram of the internal structure of the device is shown in Figure 1.

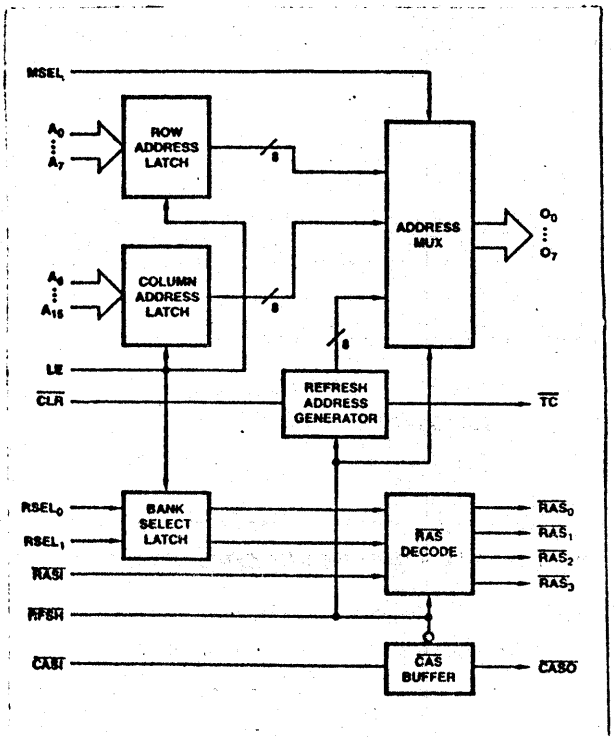


Figure 1 : Block Diagram

Six control lines are provided (among others):

RASI - Row Address Strobe input. This input is routed via a demultiplexer to the four RAS outputs to the RAM array. The demultiplexer function is determined by the RFSH input.

CASI - Column Address Strobe input. This is routed via a buffer controlled by RFSH to the RAM array.

RSELØ - RAS Select Ø/1. Used to control the RAS demultiplexer
RSEL1 in the one-of-four mode (controlled by RFSH). Normally the two highest order address bits.

MSEL - Multiplexer Select. This controls the address multiplexer to switch either the upper or lower eight address bits to the address outputs. This input is overridden by the RFSH input.

RFSH - Refresh. A low level on this input blocks the CAS signal by disabling tha CAS buffer, forces the outputs of the refresh counter onto the address outputs and changes the RAS demultiplexer from one-of-four to four-of-four.

Tables 1, 2 and 3 show the full functions of these control signals.

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

Table 1 : RAS Output Function

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

Table 2 : CASO Function

MSEL	$\overline{RFSH}$	O_0-O_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh Address

Table 3 : Address Output Function

Card Select and Buffering

The two most significant address lines A14 and A15 (A16 and A17) are buffered by spare inverters and fed to the RSELØ and RSEL1 inputs of the controller U7 and the inputs of U4, a 74LS138 connected as a a 2 to 4 line decoder with four enable inputs, two active high and two active low. Control signals VMA (Valid Memory Address) and IOS (I/O Select) from the bus are used to enable the decoder - these may be tied high if not required. The four outputs of the decoder are switched by the block enable/disable switches to a four-input AND gate to

generate the Buffer Enable signal (BEN).

The addresses enabled and disabled by the switches are shown in Table 4.

SWITCH	BLOCK	DEVICES
SW1	0000 - 3FFF (00000 - 0FFFF)	U36 - U43
SW2	4000 - 7FFF (10000 - 1FFFF)	U28 - U35
SW3	8000 - BFFF (20000 - 2FFFF)	U20 - U27
SW4	C000 - FFFF (30000 - 3FFFF)	U12 - U19

Table 4 : Block Switching

BEN is used to enable the data bus buffers U10 and U11 in conjunction with the Read Strobe and Write Strobe signals (RDS and WDS) from the bus. Two chips are used as the buffer must latch the output data from the RAM chips.

BEN is also used to force RFSH low if the 16K (64K) block has been disabled. This means that if the addressed block is disabled, two refresh cycles are performed in every memory cycle. Thus the RAM is refreshed every microsecond at least, and in come cases twice every microsecond.

The fourteen (sixteen) lower order address lines A0 - A13 (A0 - A15) are not buffered as U7 only presents one standard TTL load on its inputs.

Timing Generation and RAM Control

The bus clock Enable signal E (1MHz square wave) is used as a reference for all timing generation. As all data transfers take place during the second half of each machine cycle (E high), the first half is used to refresh the RAM array. E is thus fed to the RFSH input of the controller, and also to an edge-to-pulse converter which generates a short (30-60ns) pulse at every positive and negative transition of E. This pulse is used to trigger a chain of monostables (U3) which produce a pulse about 250ns long, occurring about 150s after each edge of E. This is used as the RASI signal for U7. It is delayed by a further 20-50ns to create the MSEL signal for U7, and after a further 20-50ns delay is ORed with RASI to generate CASI. RASI is also ORed with WDS to generate the Write Enable signal (WE) for the RAM array.

The WE, CAS, RAS0-3 and Address outputs of U7 are buffered by U8 and U9 which are 74LS244 octal buffers. These may be replaced by the plug-in compatible Am2966 RAM drivers if desired.

Construction

The board is assembled following the component overlay provided. This is approximately life-size and may thus be used to identify component holes when positioning is doubtful.

Care should be taken to solder the tantalum capacitors in the right way round. The ceramic capacitors in the RAM array are required to fit into a limited space, so the smallest possible types should be obtained. The monolithic ceramic types are best.

Once all capacitors and sockets are fitted, the board should be cleaned with alcohol and inspected with a magnifying glass for shorts or solder splashes. The impedance of the board from power to ground can be measured. A low impedance or short circuit means a faulty capacitor or shorted track somewhere.

Once the inspection is complete, insert all ICs (the right way round) and switch on. Note that if you are using separately switched power supplies, the -5V supply must come on first, followed by the +12V and then the +5V. On power down the order is reversed - +5V off first, then +12V and -5V off last. If your power supplies operate off a single switch, this sequence will not be a problem.

Should the board fail to work first time, check that all ICs are properly seated. A combination of out-of-spec monostable (U3) and large tolerance timing components (1k/10p and 4k7/100p pairs) can result in over- or underlength timing pulses - check and replace if necessary. Problems in this board are rare and are usually traced to faulty construction or poor quality components, so be careful when purchasing parts and assembling the board.

COMPONENTS LIST

Integrated Circuits

1	Am2964B	Dynamic RAM Controller (S. C. Devices)
32	4116	16K x 1 DRAM, 250ns access, 375ns cycle
	(4164	64K x 1 DRAM, 250ns access, 375ns cycle) *
1	74LS86	EXOR gates
1	74LS32	OR gates
1	74LS373	Transparent latches
3	74LS244	Non-inverting buffers
1	74LS14	Schmitt inverters
1	74LS221	Monostables
1	74LS138	3 to 8 line decoder
1	74LS21	4-input AND gates

Resistors (1/4 watt)

5	4k7
3	270R
1	1k

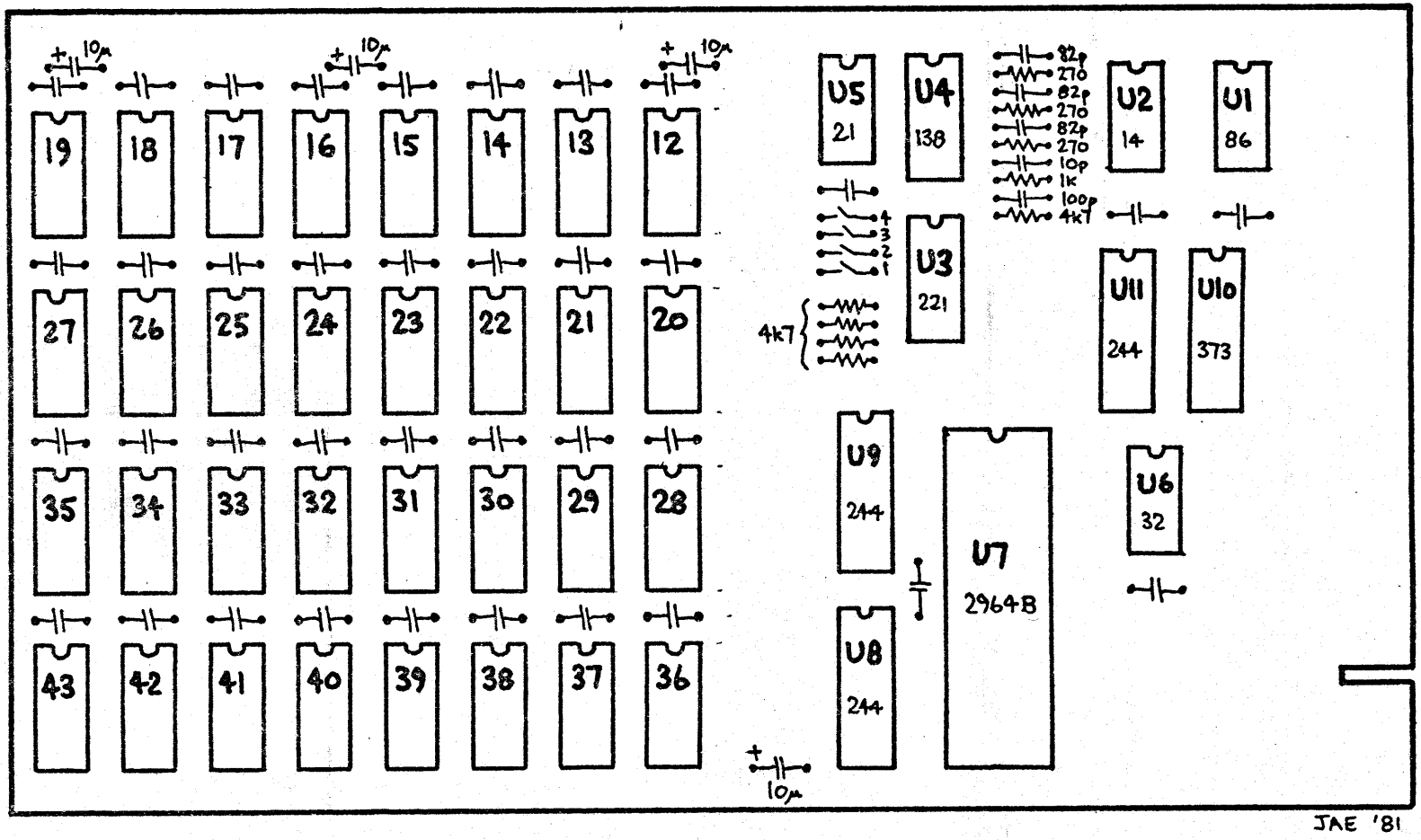
Capacitors

37	100n	ceramic
4	10u	35V tantalum
3	82p	ceramic
1	100p	ceramic
1	10p	ceramic

Miscellaneous

1	DNS-04	4-way DIL switches (or similar)
4	14-pin	IC sockets
34	16-pin	IC sockets
4	20-pin	IC sockets
1	40-pin	IC socket

* These times are for a 1MHz CPU. If it is intended to use a 2MHz CPU at a future date, it is necessary to use DRAMs with a cycle time of 250ns or less.



COMPONENT OVERLAY

NOTE: ALL UNMARKED CAPACITORS ARE 100nF

C3-BUS SERIAL I/O CARD

Jonathan Eva

Introduction

The C3Bus serial I/O card provides two asynchronous serial interface ports for a C3Bus based microcomputer. The card features two completely independent programmable asynchronous serial channels, with the baud rates of these channels being set and altered completely under software control by means of a programmable counter/timer. Provision is made for the initial (power-on) baud rate to be determined by means of switches. One channel is completely buffered to RS-232 standard levels (including control lines) while the other is buffered to both TTL and RS-232 levels. All inputs and outputs of the counter/timer are brought to a connector for external use if required. In addition, the output of the third counter may be connected to the interrupt lines of the bus if desired in order to provide a regular source of interrupts for multitasking applications.

Circuit Description

The circuit may be broken down into three parts:

i) Address decoding and card selection,
ii) Data and control buffering and PTM/ACIA interface,
iii) Channel buffering and external interfaces.

These will be dealt with separately.

1. Address decoding and card selection

Address lines A7 to A3 and control line IOS are decoded by U1 and U2 in conjunction with DIL switches A-1 to A-5 to select a single 8-byte block from the 256-byte I/O block. The decoded output from the EXOR gates (termed Card Select) is used, together with bus signal VMA, to enable U5, which is connected as a 2-4 line decoder with two active high enable inputs. U5 decodes address lines A1 and A2 and together with gates U6a and b produce the Chip Select signals for U9, U10 and U11. The gates U6a and b ensure that the PTM (U9) occupies four memory locations while the ACIAs U10 and U11 each occupy two.

The order of appearance of the PTM and ACIA registers is thus:

0 - PTM counter 0 read/load data register
1 - PTM counter 1 read/load data register
2 - PTM counter 2 read/load data register
3 - PTM control register / power-on baud rate
4 - ACIA 0 control/status register
5 - ACIA 0 data register
6 - ACIA 1 control/status register
7 - ACIA 1 data register

The card address within the 256-byte I/O block is determined by switch settings A-1 to A-5. These settings are detailed in Table I below.

A-1	A-2	A-3	A-4	A-5	Address (hex)
Ø	Ø	Ø	Ø	Ø	ØØ - Ø7
Ø	Ø	Ø	Ø	1	Ø8 - ØF
Ø	Ø	Ø	1	Ø	1Ø - 17
Ø	Ø	Ø	1	1	18 - 1F
Ø	Ø	1	Ø	Ø	2Ø - 27
Ø	Ø	1	Ø	1	28 - 2F
Ø	Ø	1	1	Ø	3Ø - 37
Ø	Ø	1	1	1	38 - 3F
Ø	1	Ø	Ø	Ø	4Ø - 47
Ø	1	Ø	Ø	1	48 - 4F
Ø	1	Ø	1	Ø	5Ø - 57
Ø	1	Ø	1	1	58 - 5F
Ø	1	1	Ø	Ø	6Ø - 67
Ø	1	1	Ø	1	68 - 6F
Ø	1	1	1	Ø	7Ø - 77
Ø	1	1	1	1	78 - 7F
1	Ø	Ø	Ø	Ø	8Ø - 87
1	Ø	Ø	Ø	1	88 - 8F
1	Ø	Ø	1	Ø	9Ø - 97
1	Ø	Ø	1	1	98 - 9F
1	Ø	1	Ø	Ø	AØ - A7
1	Ø	1	Ø	1	A8 - AF
1	Ø	1	1	Ø	BØ - B7
1	Ø	1	1	1	B8 - BF
1	1	Ø	Ø	Ø	CØ - C7
1	1	Ø	Ø	1	C8 - CF
1	1	Ø	1	Ø	DØ - D7
1	1	Ø	1	1	D8 - DF
1	1	1	Ø	Ø	EØ - E7
1	1	1	Ø	1	E8 - EF
1	1	1	1	Ø	FØ - F7
1	1	1	1	1	F8 - FF

TABLE I : ADDRESS SWITCH SETTING

NOTE : 1 = switch ON, Ø = switch OFF

The fourth memory location (PTM control / power-on baud rate) is special because two functions share the same position. The PTM control register is a write-only register, the data pins being tri-stated when a read is attempted from this location. Gates U6d and U7a detect this condition and enable buffers U8 so that the settings of DIL switches B are placed on the bus. U8 is inverting in order that a closed switch will be detected as a '1' to conform with switches A-1 to A-5.

2. Data and control buffering and PTM/ACIA interface

The data bus is buffered by U3, a bidirectional non-inverting buffer. The Direction line of U3 comes from bus line R/W

(after buffering) and the Enable line is derived from the bus clock E and Card Select via U6c.

Control lines R/W, E, RDS and WDS and address line A0 are buffered by U4 and taken to the ACIAs and PTM where required. Address line A1 is also taken to the PTM as four registers are contained within that chip which thus requires two address lines.

The interrupt outputs from the ACIAs are connected directly to bus line IRQ. These outputs may be enabled and disabled under software control. The output from the third timer of the PTM is inverted and converted to open-collector by part of U2, and may be connected to bus lines IRQ or NMI (or both!) via DIL switches A-7 and A-8 respectively.

3. Channel buffering and external interfaces

The inputs and outputs of the PTM are all connected to a header on the edge of the card. The three gate inputs (G0, G1 and G2) are pulled up via resistors to +5V in order that they may be safely left disconnected. In addition to being fed to the header the three outputs (OUT0, OUT1 and OUT2) are taken to other parts of the circuit, OUT0 and OUT1 providing the baud rates for ACIAs 0 and 1 (U10 and U11) respectively, and OUT2 being buffered and inverted by U2 to provide the programmable interrupt source.

Three clock sources for the PTM are supplied on the header. Two of these are derived from the on-board 6,144 MHz crystal oscillator (U12) by dividing it by four and sixteen via U13 to produce two clock signals of 1,536 MHz and 384 kHz. In addition, the buffered bus clock signal (1MHz) is also taken to the header.

Three power supplies (+5V, +12V and -12V) and ground appear on the header for use in external circuitry.

The inputs and outputs of ACIA 0 (U10) are buffered by 1488 and 1489 level converters (U14 and U15) to provide RS-232 compatibilty on all signals. In addition to the Transmit Data (TxD) and Receive Data (RxD) lines, control signals Data Carrier Detect (DCD), Clear To Send (CTS) and Request To Send (RTS) are buffered and taken to the header.

Power supplies of +5V, +12V and -12V are included, as well as two pins passively pulled to +12V and -12V. These are intended to be used to tie unused control signals to their required states.

The interface of ACIA 1 (U11) is more complex as it is intended that this may be used with RS-232 or TTL levels as desired.

All signals (TxD, RxD, DCD, CTS and RTS) are buffered to TTL levels by U16, a hex Scmitt inverter. In addition, TxD and RTS are buffered to RS-232 levels by U14c and d. A non-inverting RS-232 to TTL level converter (U15d and U16f) is provided in

order that the incoming RxD signal may be converted to TTL levels before being applied to the RxD input of the ACIA.

Power supplies of +5V, +12V and -12V are again provided. Unused control inputs (CTS and DCD) may be tied directly to +5V or ground as required.

Construction and setting up

The component layout is, as always, actual size. No constructional problems should be encountered.

The crystal used does not have to be exactly 6,144 MHz - any close frequency may be used, but this must be taken into account when calculating the frequency division factors. Link the CLKØ and CLK1 pins on the PTM header to the appropriate clock source (see below) if you want any baud rates to be generated!

The actual power-on baud rate setting may be achieved in a number of ways. The settings of DIL switches B are not related in any physical way to the PTM, but merely provide a means of getting presettable information into the system. Thus it is possible to encode baud rates, i.e. make a switch setting of Ø1 (ØØØØØØØ1) mean 11Ø baud, Ø2 mean 3ØØ baud etc. with the actual division factors being held in a table in ROM. It would be possible to preset up to 256 different baud rates in this way.

A better method is to make the switch settings correspond to the actual division factor itself. Since only eight bits may be preset, it is convenient to make these correspond to the lower eight bits of the count value and assume the upper eight bits to be zero. Thus on power-up it is only necessary to read the switches and copy the value straight into the PTM. This method means that the maximum division factor possible is 255, so the clock frequency to the PTM must be suitably selected. It is usual to generate a 16x baud rate frequency for the ACIAs.

As an example, assume that you wish the power-on baud rate to be 11Ø baud. The desired frequency is thus 16x11Ø = 176Ø Hz. Using the 1,536 MHz clock means a division factor of 873, which is too large. Using the 384 kHz clock reduces the division factor to 218 (11Ø1Ø1Ø binary) which is set on DIL switches B (B-8 is the MSB, B-1 the LSB).

If 96ØØ baud is required (i.e. a frequency of 96ØØx16 = 153,6 MHz) then the 384 kHz clock is too low, so the 1,536 MHz clock is used with a division factor of 1Ø (ØØØØ1Ø1Ø).

COMPONENTS LIST

Integrated circuits

2	74LS136	O-C EXOR gates
1	74LS245	Bidirectional buffers
1	74LS367	Hex buffers
1	74LS138	3-8 line decoder
1	74LS00	NAND gates
1	74LS32	OR gates
1	81LS96	Inverting bufers (may also use 81LS95)
1	8253	Programmable Timer Module
2	6850	ACIAs
1	74S04	Inverters (may also use 74LS04)
1	74LS93	Counter
1	1488	RS-232 line driver
1	1489	RS-232 line receiver
1	74LS14	Hex Schmitt trigger

Resistors

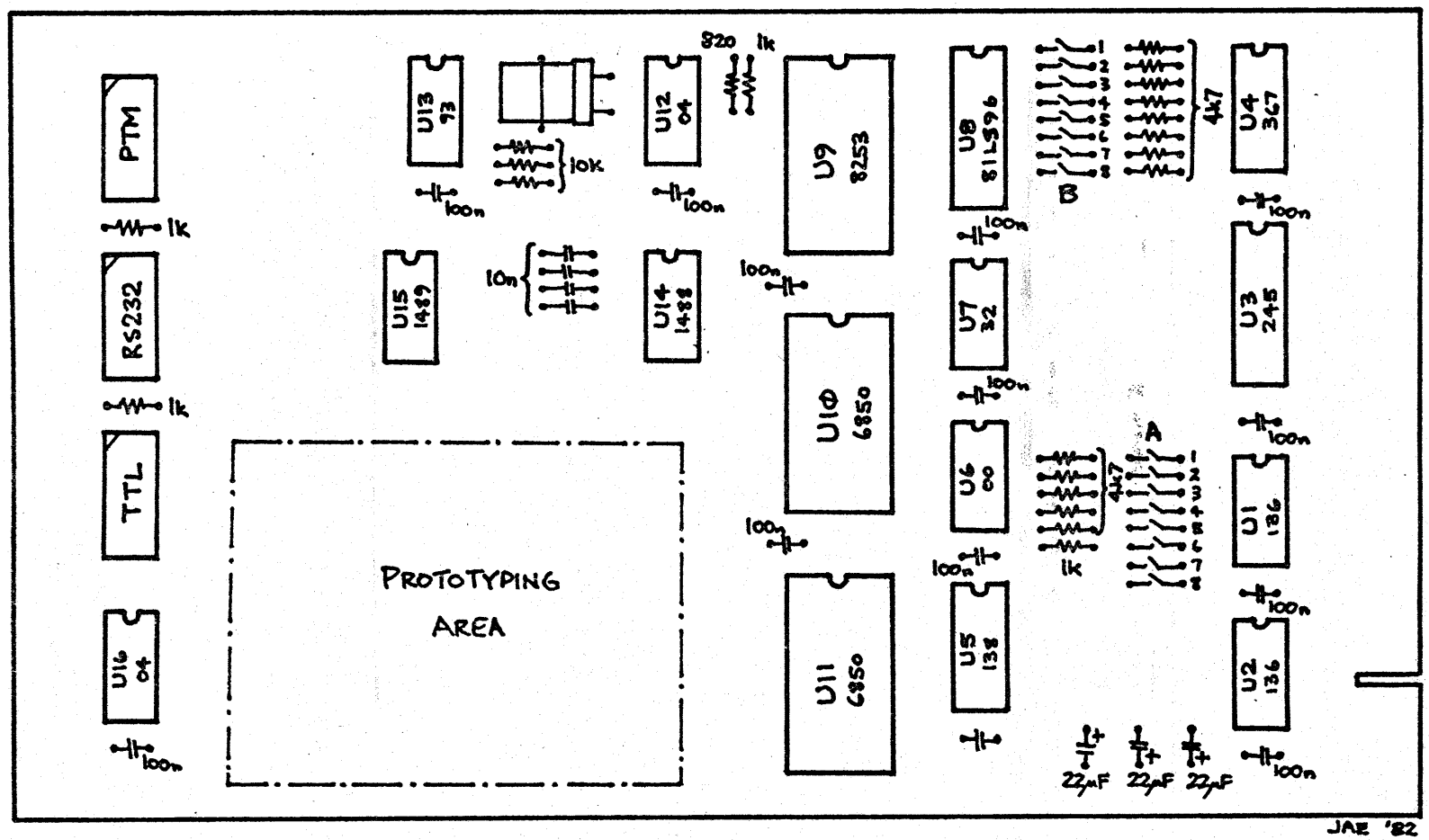
1	820R	1/4W 5%
4	1k	" "
4	2k2	" "
13	4k7	" "
3	10k	" "

Capacitors

13	100n	ceramic
3	22u	tantalum

Miscellaneous

2	8-way	DIL switches
1	6,144 MHz	crystal
9	14-pin	IC sockets
5	16-pin	" "
2	20-pin	" "
3	24-pin	" "



COMPONENT OVERLAY

C3BUS PARALLEL I/O CARD

Jonathan Eva

Introduction

The C3Bus parallel I/O Card is designed to allow a number of peripheral devices to be interfaced to a C3Bus based computer via parallel ports. There is a total of 80 I/O lines available, made up of eight individual ports of eight bi-directional data lines and two control lines each. In addition, provision is made for a real-time clock/calendar chip to be included on the card which will connect to eleven of the I/O lines. Battery backup (two PX625 mercury batteries) is provided, and the rest of the available card space is laid out as a wire-wrap/prototyping area.

Circuit Description

Four MC6821 Peripheral Interface Adapter chips (U6, 7, 8 and 9) are used to provide the parallel interface lines. Each of these chips contains six internal registers (three per port) - CRA (Control Register A), PRA (Peripheral Register A), DDRA (Data Direction Register A), CRB, PRB and DDRB. Of these six, PRA and DDRA occupy the same address as do PRB and DDRB. Access to these pairs of registers is controlled by bit 2 in the appropriate Control Register. Each PIA thus occupies four memory locations.

Memory decoding for the board is provided by U3, four open-collector EXOR gates, in conjunction with DIL switches A. These decode sixteen consecutive locations to produce an active-high Card Select signal. This signal is used together with the bus signals VMA and IOS to enable U2 which decodes A3 and A2 into four separate Chip Select signals, one for each PIA. The address selection is given in table I.

The sixteen PIA registers appear in the following order:

0 -	PIA 0 (U6)	PRA/DDRA
1 -		CRA
2 -		PRB/DDRB
3 -		CRB
4 -	PIA 1 (U7)	PRA/DDRA
5 -		CRA
6 -		PRB/DDRB
7 -		CRB
8 -	PIA 2 (U8)	PRA/DDRA
9 -		CRA
A -		PRB/DDRB
B -		CRB
C -	PIA 3 (U9)	PRA/DDRA
D -		CRA
E -		PRB/DDRB
F -		CRB

The remaining address lines A1 and A0, and bus signals R/W, Reset and Clock are buffered by U1 and passed to the PIA chips. The data lines D0-D7 are buffered by U5, an octal bi-directional buffer whose direction line (Dir) is controlled by R/W. The bus Clock signal is gated with Card Select by U4 to produce the Enable signal for U5.

Interrupt Switching

Each PIA has two interrupt outputs, IRQA and IRQB, which are active-low, open-drain outputs. For different applications it may be desirable to connect either or both (or neither) of these signals to the IRQ or NMI bus lines. DIL switches B and C allow any combination of the eight PIA interrupt outputs to be connected to the IRQ and NMI control lines. Switching details for this is given in table II.

The Real Time Clock/Calendar

The Real Time Clock chip (RTC) used is the OKI MSM5832 which provides registers for Year, Month, Day, Day of Week, Hours, Minutes and Seconds. Twelve or twenty-four hour notation is catered for, and provision is made for leap years. Standby supply voltage may be as low as 2,2V and the clock uses a standard 32768Hz watch crystal. Four interrupt rates are provided - every 1/1024th second, every second, every minute and every hour.

Four data lines, four address lines and four control lines form the interface to the chip. The addresses of the different registers are given in table III.

Because of the slow operation of the chip, it is necessary to access it through a PIA. The four data lines are brought to the least significant bits (bits 0-3) of port A on PIA 0, while the address lines are taken from bits 0-3 of port B. Bits 4, 5 and 6 of port B are used for the Read, Write and Hold control lines.

Interrupts from the RTC appear on the data lines when A0-A3 are high. These are switched via DIL switches D to the CA1 control line on PIA 0. Note that not more than one of these switches should be closed at any time, as this will result in errors when reading from and writing to the RTC. Switching details for D are given in table IV.

Battery backup for the RTC is provided by B1 and B2, two PX625 or similar 1,35V mercury cells. Current flow from these is controlled by D1 and D2. D3 ensures that the Chip Select input to the RTC is held slightly below Vcc when power is on to prevent damage to the RTC.

Construction

Assembly of the board should follow the component overlay in Figure 1. Note that this is actual size and may be used to determine component positions when doubtful. The mounting of

the backup batteries is up to you - two fastening holes are provided on either side of the contact pads for this purpose. Some form of battery holder should be constructed as soldering directly to the batteries is difficult, possibly dangerous and certainly doesn't improve their life.

The four rows of terminal points for connection to the PIAs have been drilled slightly larger to allow wire-wrap pins or other types of terminations to be inserted. If you are going to connect to these holes more than once, some type of terminal is ESSENTIAL - they will not stand repeated soldering and desoldering.

If you are going to use the RTC, remember to insert the twelve links required to connect it to PIA Ø!

TABLES

A-1	A-2	A-3	A-4	Card Address
Ø	Ø	Ø	Ø	ØØ-ØF hex
Ø	Ø	Ø	1	10-1F hex
Ø	Ø	1	Ø	20-2F hex
Ø	Ø	1	1	30-3F hex
Ø	1	Ø	Ø	40-4F hex
Ø	1	Ø	1	50-5F hex
Ø	1	1	Ø	60-6F hex
Ø	1	1	1	70-7F hex
1	Ø	Ø	Ø	80-8F hex
1	Ø	Ø	1	90-9F hex
1	Ø	1	Ø	A0-AF hex
1	Ø	1	1	B0-BF hex
1	1	Ø	Ø	C0-CF hex
1	1	Ø	1	D0-DF hex
1	1	1	Ø	E0-EF hex
1	1	1	1	F0-FF hex

TABLE I : CARD ADDRESSING

NB: 1 = Switch ON, Ø = Switch OFF

Switch #	PIA #,line
1	Ø,IRQA
2	Ø,IRQB
3	1,IRQA
4	1,IRQB
5	2,IRQA
6	2,IRQB
7	3,IRQA
8	3,IRQB

TABLE II: PIA INTERRUPT SWITCHING

NOTE - DIL switch B connects the eight PIA interrupt lines to bus line IRQ according to the above table. DIL switch C connects the PIA interrupt lines to bus line NMI in the same way.

Addr Inputs A0	A1	A2	A3	Internal Counter	Data I/O (4) D0	D1	D2	D3	Data Limits	Notes
Ø	Ø	Ø	Ø	S 1	*	*	*	*	Ø - 9	(1)
1	Ø	Ø	Ø	S 1Ø	*	*	*		Ø - 5	(1)
Ø	1	Ø	Ø	MI 1	*	*	*	*	Ø - 9	
1	1	Ø	Ø	MI 1Ø	*	*	*		Ø - 5	
Ø	Ø	1	Ø	H 1	*	*	*	*	Ø - 9	
1	Ø	1	Ø	H 1Ø	*	*	#	#	Ø - 1/2	(2)
Ø	1	1	Ø	W	*	*	*		Ø - 6	
1	1	1	Ø	D 1	*	*	*	*	Ø - 9	
Ø	Ø	Ø	1	D 1Ø	*	*	#		Ø - 3	(3)
1	Ø	Ø	1	MO 1	*	*	*	*	Ø - 9	
Ø	1	Ø	1	MO 1Ø	*				Ø - 1	
1	1	Ø	1	Y 1	*	*	*	*	Ø - 9	
Ø	Ø	1	1	Y 1Ø	*	*	*	*	Ø - 9	

Notes:

(1) S1 and S1Ø are reset to zero irrespective of input data DØ to D3 when write instruction is executed with address selection

(2) D2='1' for PM, 'Ø' for AM
D3='1' for 24 hour format, 'Ø' for 12 hour format

(3) D2='1' for 29 days in month 2, 'Ø' for 28 days in month 2. If D2 previously set to '1', on completion of month 2 day 29, D2 will be internally reset to 'Ø'.

(4) * = data valid as 'Ø' or '1'
= data bits used for AM/PM, 12/24 hr and leap year
= data bit unused ('Ø' during a read)

TABLE III : REAL TIME CLOCK REGISTERS
(From MSM5832 Data Sheet)

SWITCH	FREQUENCY
D-1	1Ø24 Hz
D-2	1 Hz
D-3	1/6Ø Hz
D-4	1/36ØØ Hz

TABLE IV : RTC INTERRUPT FREQUENCIES

NOTE : Close appropriate switch for desired interrupt frequency

COMPONENTS LIST

Integrated Circuits

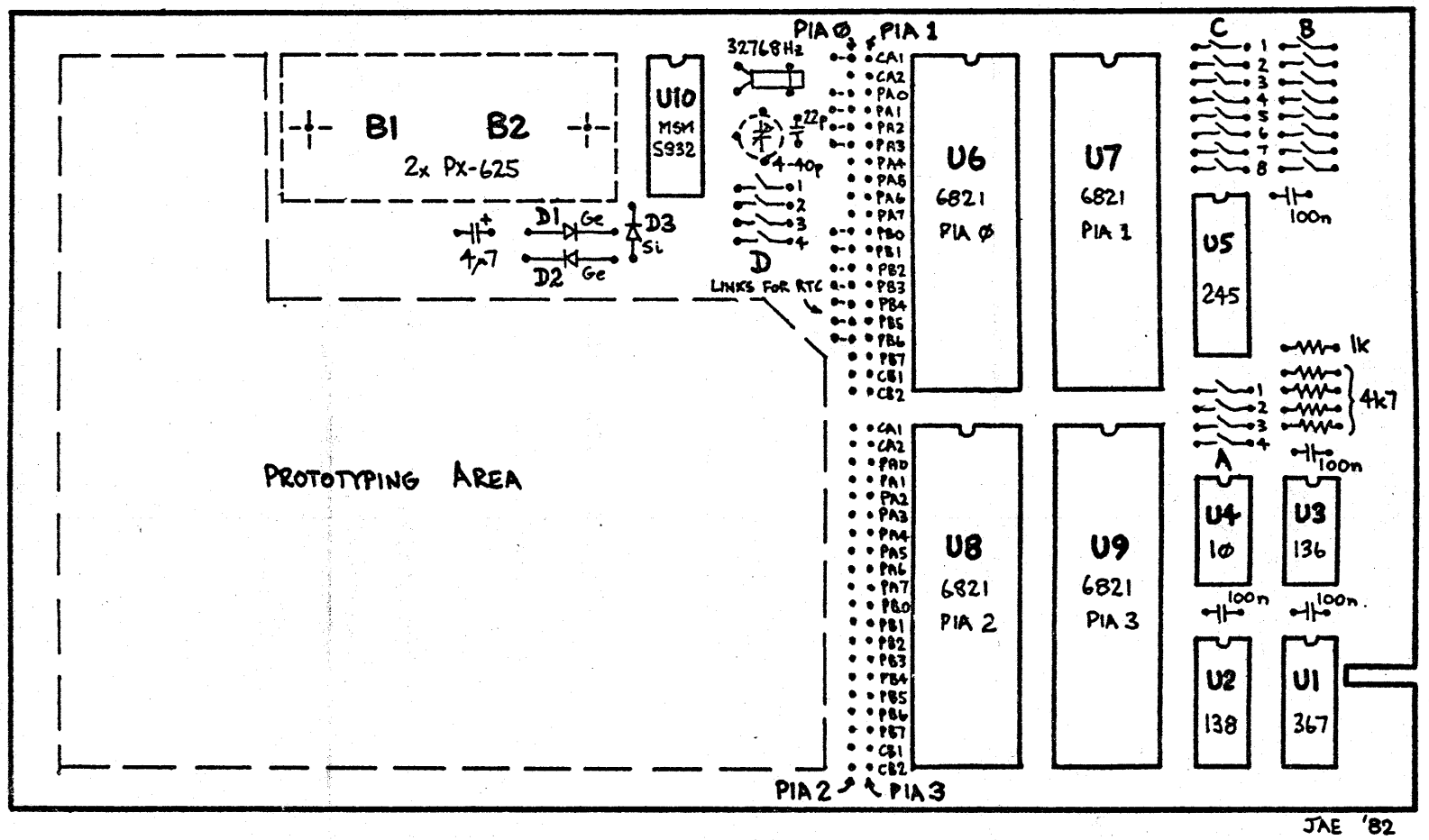
4	MC6821	PIAs
1	74LS136	Open-collector EXORs
1	74LS138	3-to-8 line decoder
1	74LS367	Hex buffer
1	74LS10	NAND gates
1	74LS245	Octal buffer
1	MSM5832	Real-time clock/calendar (Radiokom)

Discrete Components

4	4k7	1/4W resistors
1	1k	" "
4	100n	Ceramic capacitors
1	22p	" "
1	2-40p	Trimmer capacitor
1	32768Hz	Crystal (Radiokom)

Miscellaneous

4	40-pin	IC sockets
1	20-pin	" "
1	18-pin	" "
2	16-pin	" "
2	14-pin	" "
2	DNS-08	8-way DIL switches
2	DNS-04	4-way DIL switches



COMPONENT OVERLAY

C3-BUS CRTC AND VIDEO RAM CARD

Neil Walsh

Introduction

The C3-BUS CRTC and VRAM card was designed to provide the 68Ø9 Microsystem with an integrated console and also the ability to display low resolution graphics and symbols. There is an expansion connector on the board to permit the future addition of external high resolution or other attribute cards. The board combines the advantages of a normal port addressed terminal and that of memory mapping. The board need not appear on the bus or affect the normal memory map, but can be made to mimic a programmable block of memory like a normal memory-mapped VDU. The character generator can be altered by software and has to be loaded by firmware after the initial power-up of the board.

Overview

The CRT Controller and Video RAM card, or CRTC and VRAM card, contains 8K of fast static RAM which is organised into two separate 4K blocks. These two blocks are called the text RAM and the generator RAM, and perform the following functions:

The text RAM contains the actual pattern of characters that appears on the screen. Each character is represented by a single byte (8 bits), so it follows that a screen layout of (say) 16 lines of 72 characters per line will need 16x72 or 1152 locations to hold it. It will ALWAYS need 1152 locations, since a space or blank is also a character! It also follows that there can be up to 256 different characters on the screen at any time (8 bits = 256 combinations) but no more.

The generator RAM holds the pattern of dots that makes up each character. A typical character will be made up out of a matrix of 7x9 dots, 7 horizontal and 9 vertical, and this matrix would be stored in 9 successive bytes in the generator RAM. Because there is 4K of generator RAM for 256 characters, it can be seen that each character can have up to 16 lines vertically. The horizontal width is limited to 8 dots by the size of the byte.

Normally a large amount of logic is required to control the accessing of these RAM blocks. In this case, it has been largely simplified by the use of a special CRT controller chip, the Motorola MC6845, which can be programmed to generate the addresses needed to provide the display. Further logic is required, however, to control access by the system to the RAM and to regulate the data flow within the circuit.

Circuit Description

(Refer to Sheet 1)

The master dot clock (DCLK) is generated by inverters from U28. The nominal frequency used in the standard configuration is

14,2 MHz. This clock is divided down, usually by 8, to give the character clock frequency (CCLK). This is because there are normally 8 dots per character. The divider counter circuits comprise U29, U33 and a U30 gate. However this counter can optionally divide by 6 if the FORM bit (bit 1) of register U43 is not set (i.e. low). The output of the divider circuit is a square wave which is used to time the CRTC chip U42 and the VRAM memory accesses.

The main memory decoding is done by U2, U34 and U44. The addresses decoded by this section of the circuit correspond to the memory map addresses that the VRAM will respond to. If the character generator is enabled by bit 0 of register U43 (GENE) then the 4K of character generator RAM will respond to the physical addresses $B000-$BFFF. The memory can only be written into but as this will usually overlay normal system memory, read/write access is possible. If the GENE bit of register U43 is set, the character generator RAM is write-protected, and the system memory at address $B000-$BFFF can be used as normal without affecting the character patterns on the screen.

The text block of VRAM can respond to any 4K block of memory addresses. The actual address that it will respond to is determined by the bits b4 - b7 of register U43. The output of comparator U44 will become true if the physical 4K address on the system bus corresponds to those bits of register U43. As with the character generator RAM, the text portion of the VRAM can only be written to and not read. As it is usually occupying the same address as normal system memory, however, read/write access of screen text is possible since a write to the VRAM will write to both VRAM and normal system RAM but a read will only read from the system RAM. Because the timing of the video RAM (VRAM) is not synchronised to the main system timing, the memory request signal MRQ has to be latched into flip flops U39 and U33 until the CRTC timing is ready.

As mentioned earlier, the actual VRAM access is timed by the character clock (CCLK). The VRAM must be read once per CCLK cycle by the CRT controller in order to maintain the character display on the screen. Frequently, however, the system will also require access in order to update or alter the screen display. When this happens the CCLK cycle has to be split into two. When CCLK is low the latched system bus can have access but during the high half of CCLK the CRTC (U42) must control the VRAM address and data lines in order to prevent visible abnormalities ("snow" and glitches) appearing on the screen. Once the memory request signal MRQ is latched into U39 and U33 and CCLK has gone low, flip flop U39 will activate the GRNT signal which will switch over the address and data lines of the selected VRAM block (text or generator) to the latched system bus. When CCLK goes high again, the CRTC reqires the VRAM lines and therefore both flip-flops in U39 have to be reset to switch the VRAM address and data lines back. The two gates of U38 are used to decode the GRNT line so that a write strobe is only generated for the required VRAM block. Note that if the text RAM is placed at the same address as the generator RAM ($B000-$BFFF) then the text RAM gets priority and the generator RAM is automatically disabled.

Because the dots come out of the generator RAM in parallel, 8

bits at a time, these have to be converted to serial format by shift register U35. U32 is used to decode the terminal count of the the CCLK divider to derive the parallel load signal PLOAD. This signal will go low for just the last half of the dot clock (DCLK) on the last dot of the character. This signal is used to simultaneously load all eight bits of the data pattern from the generator RAM into shift register U35, which will present them one bit a time to the video interface circuit. The shift register U35 is clocked by DCLK.

MOS RAM chips are fairly slow and need time to provide their data. The 6845 CRTC chip will provide a refresh address at the start of the line and immediately indicate that the display should be enabled with the DISEN signal. However, the RAM chips will not be ready and invalid data will be latched into the shift register U35. To prevent the unwanted display of these invalid characters, the display must be blanked for an additional period which will be an integral number of CCLK cycles.

Because the data coming out of the generator RAM is latched twice, first into U31 (sheet 3) and then into register U37, it is necessary to delay the blanking of the screen by two CCLK periods. Two D-type flip-flops in U37 are used to pipeline the DISEN signal so that it is delayed by two CCLK cycles. Because all the screen characters are in fact being displayed two cycles late the cursor signal CUR from the CRTC (U42) has to be delayed in a similar manner using the other half of U37. To avoid logic racing problems the PLOAD sigal is inverted and used to clock U37 instead of using CCLK. U36 is used to invert the video dots during the cursor display. A gate of U34 is used to mix the horizontal and vertical sync signals from the 6845 CRTC before the final mix with a transistor circuit giving a 1 Volt peak-peak composite video signal.

IC's U2, U3, U32 and U38 are used to decode the lower 8 bits of the address bus together with the IO Select signal to select either the CRTC U42 or the control register U43 (which is write only). The signals provided are DBUFE to enable U11, CRTCS to select the 6845 and the Latch Enable signal for U43. The control register is selected by a write to IOBASE+$FC or $FD while the CRTC U42 responds to accesses to IOBASE+$FE and IOBASE+$FF, where IOBASE is the base address of the 256-byte IO page decoded by the IOS signal.

(Refer to Sheet 2)

The circuitry on this page covers the video memory which holds the actual character codes, which are usually ASCII, and are displayed on the screen as text. This video RAM is referred to as text RAM. Because the screen of a normal monitor or TV set is continuously scanned to maintain the display, the text RAM block has to be sequentially and repetitively read to achieve this. The 6845 CRT controller chip U42 will automatically provide the correct sequential addresses provided it is correctly programmed. It will also generate the synchronising signals (called VER and HOR) that control the vertical and horizontal retrace.

There are 16 registers in the 6845 which program the behaviour of the chip. Two of these registers together contain the cursor address. When the text RAM refresh address from the 6845 is the same as the cursor address register then the CUR signal from U42 is enabled and causes the display logic to invert the video level. The display enable signal from U42 will cause the display logic to blank the video signal during CRT beam retrace.

There are also various system signals that have to be used to control and access the 6845. These are the system data bus DØ-D7 which is buffered by U11, the 1MHz E clock and the Read/Write signal R/W. The generation of the chip select signal CRTCS, the data buffer enable signal DBUFE and the character clock CCLK are covered in sheet 1.

The text RAM consists of U12-U19 which are 1K x 4 bit static memory chips (2114). The address lines of these RAM chips can be derived from one of two sources. When the GRNT signal is not active (high), which is the normal case, U40 and U41 are enabled and the addresses are provided by the CRTC for refresh. When the GRNT is active then these two tri-state buffers will be switched off and U6 and U8 will be enabled. The system bus will then provide the access address. Because it is unlikely that the VRAM will be able to respond immediately, the system address bus and data bus contents are latched by the MRQ signal. The latches U6, U8 and U10 need not wait very long because the VRAM is ready at least every 660 nanoseconds - corresponding to one CCLK cycle. WR2 which was generated by U38 on sheet 1 will cause an orderly write to the text RAM at the correct time.

The RAM chips U12-U19 are normally in the read mode and the data they provide is available to the character generator circuitry on sheet 3. When they are in the read mode (when GRNT is not active) the system data bus latch U10 and address latches U6 and U8 are disabled to avoid contention.

The signals RØ-R3 comming from CRTC-U42 will tell the character generator circuitry which vertical slice of the character being refreshed is to be displayed. This is of course relative to the actual line that the CRT beam is scanning at that time.

The actual RAM chips that are being accessed at any time by either the bus latches or CRTC have to be decoded by U4. This will select any 1 of the 4 pairs of RAM according to the required address. Because the RAM chips are only half a byte wide 2 chips have to paired to obtain 1K bytes of memory.

(Refer to sheet 3)

This circuit covers the character generator memory section. In the normal mode during screen refresh, the text RAM on sheet 2 provides a stream of ASCII codes representing the characters on the screen. The data from the text RAM is latched into U31 on the rising edge of CCLK so that the address to the generator RAM will remain stable for a full CCLK cycle. The 8 bits from U31 select one of 256 possible characters. Since a normal font

uses 128 characters, it is thus possible to store two complete and different fonts in the generator RAM.

The 4 least significant address lines of the generator RAM select which one of the 16 vertical rows of the character selected by the text RAM is being displayed. These row address lines, which originate from the CRTC on sheet 2, are buffered by half of U41. During the period that an access is being made by the address and data latches linked to the system bus, U41 and U31 are switched off to avoid contention.

The address lines of the generator RAM chips U20-U27 are controlled by either the character selection lines from U41 and U31, or the system address bus latches U5 and U7. The switching between the two sources is controlled by the grant (GRNT) signal from sheet 1. Because the timing of the write access has to be made when the generator RAM is not being required by the refresh circuitry, write access is made in the same manner as for the text RAM chips. The system address and data bus lines are latched to U5, U7 and U9 if the generator RAM is write-enabled (by U43 bit 0) and the correct memory address is present on the bus. When the control logic on sheet 1 determines that transparent access can be made the GRNT signal switches the buffers over and an orderly WR1 signal is generated.

Note that all registers U5-U10 are simultaneously latched if either the text or generator RAM is required. However, only the required WR1 or WR2 signal will be generated to enable writing to the relevant RAM bank.

The second half of U4 is used to determine which of the 4 possible generator RAM chip pairs is selected when the generator RAM is accessed.

Glossary of Mnemonics

A0-A15	System address bus.
D0-D7	System data bus.
MW	System memory write strobe.
R/W	System data bus direction control (Read/Write).
IOS	Predecoded address of IO page in system memory map.
E	1MHz main system timing clock.
DCLK	Dot clock. The frequency of this clock determines the width and ultimate number of dots on the screen (nominally 14,2 MHz). This therefore controls the shift register which outputs the dots to the screen.
CCLK	Character clock. This is the dot clock divided by the width of a character in dots. This is the frequency at which the VRAM has to be read during normal screen refresh. The inverse signal CCLK is used to latch the data from the text RAM to the generator RAM.
PLOAD	Parallel load. A short low going pulse which occurs at the end of each character display period to load the 8 bit pattern from the character generator into the shift register to be converted to serial form.
MRQ	Memory request. This signal determines that a valid VRAM address has appeared on the system bus. It is used to latch the system address and data bus and to initiate the access logic.
GRNT	External access grant. When this line goes high all the normal (refresh) address and data lines to the VRAM chips are disconnected ready for an external access. The inverse signal GRNT is used to enable the external address and data latch buffers of both VRAM blocks ready for an external write.
WR1	Generator write strobe. This goes to the write enable of the character generator RAM chips.
WR2	Text write strobe. This goes to the write enable of the text RAM chips.
GD0-GD7	Generator data. These are data lines coming out of the character generator RAM ready to be converted to a serial stream of dots by the shift register.
TD0-TD7	Text data. These data lines come from the text display RAM and are latched into the character generator code select buffer.
R0-R3	Row addresses. These lines come from the CRT controller chip and indicate to the character generator logic which particular line of the selected characters is to be displayed.
HOR	Horizontal sync timing. This is the line synchronisation signal required by the monitor or TV set.
VER	Vertical sync timing. This is the vertical synchronisation signal for the monitor.
CUR	Cursor display. A control signal generated by the CRTC chip to enable the display of the cursor at its required position on the screen.
DISEN	Display enable. This signal is generated by the 6845 CRTC chip to blank the CRT beam during vertical or horizontal retrace.
LPEN	Light pen. This is an input into the CRTC available for future expansion to indicate the presence and position of a screen light pen.
RES	Reset. This signal can be used by external expansion

logic to clear and presynchronise the CRTC counters.

CRTCS — Chip select for CRTC. Decoded chip select line.

DBUFE — Data buffer enable. This signal enables the data bus buffer between the CRTC and the system.

VID — Video. TTL level signal which indicates the state (on/off) of the CRT beam.

MSYN — Mixed sync. TTL level indicating that the CRT is to perform horizontal or vertical retrace. The CRT differentiates between the two by the length of the sync pulses.

MVID — Mixed video. Composite 1 Volt p-p video signal for output to the monitor.

Programming Considerations

To assist with the setting up of the 6845 CRTC a short initialisation routine is provided. For those requiring a fuller explanation of the chip it is recomended that the reader get hold of a copy of the CRT Controller Handbook by Gerry Kane, or the Motorola data sheet on the MC6845.

The first register appearing at IOBASE+$FE is an address register. If this has ØØ to $11 written into it the appropriate one of 18 internal registers can be accessed. The selected register will then appear at address IOBASE+$FF in the system. It is only necessary to program the first 16 to initialise the screen display. The last two contain data relevant to the light pen interface. Because the 68Ø9 microprocessor has a 16 bit accumulator (registers A and B joined) it is convenient to set up the address register and register contents simultaneously with just one store instruction.

```
                * INITIALISATION OF CRT CONTROLLER

                CRTC    EQU     $EØFE     IOBASE+$FE

8E  C1ØF  INZVDU LDX     #TABLE    programming constant table
4F                      CLRA               select CRTC register #Ø
E6  8Ø    INZ    LDB     Ø,X+      select constant value
FD  EØFE         STD     CRTC      write A then B to CRTC
4C                      INCA               select next CRTC register
81  1Ø           CMPA    #16       last register programmed?
25  F6           BLO     INZ       no: carry on
39                      RTS                return

                * CONSTANT PROGRAMMING TABLE:
                * NOTE : ASSUMED DCLK FREQUENCY IS 14,1926 MHz
                *          8 DOTS PER CHARACTER

                TABLE   EQU     *
71              HORTOT  FCB     113       characters per line - 1
5Ø              HORDIS  FCB     8Ø        no. of displayed chars
5C              HSYPOS  FCB     92        position of HOR sync
Ø8              HORWID  FCB     8         width of HOR sync pulse
1B              VERTOT  FCB     27        char rows on screen - 1
Ø4              VERADJ  FCB     4         vertical adjustment value
18              VERDIS  FCB     24        displayed character rows
```

```
19      VSYPOS  FCB   25      position of VER sync pulse
ØØ      INTERL  FCB   Ø       interlace mode
ØA      MXSADR  FCB   1Ø      lines per character - 1
Ø9      CURSTR  FCB   9       first line of cursor
ØA      CUREND  FCB   1Ø      last line of cursor
BØØØ    STARTH  FDB   $BØØØ   start of screen RAM
BØØØ    CURSOR  FDB   $BØØØ   cursor position address
```

Loading of the Character Font

To permit the loading of a character font, the generator RAM must be enabled and therefore bit Ø of the VRAM control register U43 must be clear. Another point to bear in mind is that the text RAM must not reside at $BØØØ-$BFFF when the character generator is being loaded - therefore the control register bits 7 to 4 must contain some value other than 1Ø11 (hex B).

To help you find the actual address of a character when the font is loaded into memory the following guideline should be useful:

The ASCII character 'A' has the hex code $41. The start of the character pattern can thus be found at $B41Ø. The two centre digits correspond to the ASCII character code in hex. The 16 bytes starting at this address are the patterns required to generate the dots for the row lines starting at the top of the character and working down.

When a bit in the generator RAM is logic 1 it means that the beam must be made bright for that dot, and dark (black) if the bit is Ø. All rows of zeroes in the character font correspond to the gaps between lines and characters.

The ASCII character 'Z' for instance is hex $5A, so its pattern can be found at $B5AØ when the generator RAM is enabled and the font loaded.

Normally the font is automatically loaded from a compressed pattern in the startup firmware monitor and the user need not worry about having to do this. Different fonts can be loaded from disk or tape when they are required. After loading the font the loader routine should set bit Ø of the control register to logic 1 to disable the character generator. Once the system has done this and taken memory block $BØØØ-$BFFF for its own use the original font pattern remains in the actual character RAM but cannot be read or written.

Setting the Text RAM Response Address

The text RAM can be programmed to respond to any 4K block of memory addresses to make screen editing and fast screen display routines possible. The address of the screen text can thus also be moved to a convenient location when different memory is required by the users software. If one wanted the screen work area to be at $9ØØØ-$9FFF one would have to write a hex 9 into the top 4 bits of the response (control) register at

IOBASE+$FC, i.e. the top 4 bits correspond to the desired values of A15-A12 on the address bus.

Another point to bear in mind when setting up this register is that b1 must be set to logic 1 if you are using eight dots per character. If this is incorrectly set then the dot patterns and scanning will be jumbled giving an unreadable screen. Bit b0 will usually be set to logic 1 as well, to prevent the character generator from being overwritten and also rendering unreadable screen. Therefore to follow the above example hex $93 should be written to the register at IOBASE+$FC.

Control Register Bit Functions

b0 - generator enable	0 = enable write to generator RAM 1 = protect generator overwrite
b1 - character width	0 = 6 dots wide (for 5x7 format) 1 = 8 dots wide (for 7x9 format)
b2 - frequency select	(off board clock select)
b3 - attribute enable	(off board interface)
b4 - A12	address bus selection
b5 - A13	" " "
b6 - A14	" " "
b7 - A15	" " "

Construction

Assembly of the CRT controller board is started by following the full size component overlay provided. Because of the high component density of the board it is recommended that thin high quality solder and a narrow tip iron are used to solder in sockets and components. An insulating pad should be laid under the crystal to isolate it from the tracks on the board.

After soldering the board it should be cleaned with isopropyl alcohol and examined with a magnifying glass to check for solder splashes or dry joints.

The 44 ICs should then be located and inserted into their sockets.

After the monitor has been connected and the board installed into the system powerup should bring immediate success. If the monitor does not lock into the signal then the vertical and horizontal hold controls may need to be adjusted. The brightness and contrast controls will also need adjusting to get a good picture.

If the display does not provide any video signal at all, the first check-point is to make sure that the master dot clock is oscillating. A 74S04 chip in position U22 will always render a good clean clock signal at 14,2 MHz. If, however, a standard TTL chip (7404) was used it may be necessary to select another

chip to get good results.

Uneven size dots on the screen or unwanted flickering dots may indicate that shift register U35 is not meeting specification and could need replacing. With a scope CCLK and DCLK can be looked at together. DCLK should be 6 or 8 times higher that CCLK if the divider circuits are working. The PLOAD signal should also appear and is identified as a single low going pulse just before the falling edge of CCLK.

If the wrong characters consistently appear on the screen then there may be a short or open connection to the address or data lines of the text RAM. Consistently misformed characters may be caused by similar problems with the character generator RAM. If there are no shorts or open lines then there may be a bad or slow RAM chip installed.

Good careful construction has brought about immediate success on all boards constructed so far, so the above checks are well worth it. Make sure that there is not a low resistance reading between +5V and ground. A blown chip or board short can cause this.

A fast switching transistor like the 2N2222 should be used to get a good video output.

Expansion Header Connections

PLOAD - 1	16 - GND
DCLK - 2	15 - GND
CCLK - 3	14 - GND
TD7 - 4	13 - ATTE
HOR - 5	12 - FREQ
VID - 6	11 - LPEN
VER - 7	10 - RESET
MVID - 8	9 - DISEN

Note: the normal connection straight to a monitor is made between pin 8 and pin 16 (GND).

COMPONENTS LIST

Integrated Circuits

16	2114 1Kx4 RAM (250ns)
5	74LS374
2	74LS373
1	74LS377
1	74LS244
2	74LS245
2	74LS00
1	74LS02
2	74LS20
1	74LS30
1	74LS32
1	74LS73
2	74LS74
1	74LS85
1	74LS86
1	74LS139
1	74LS165
1	74LS175
1	74S04
1	MC6845

Resistors

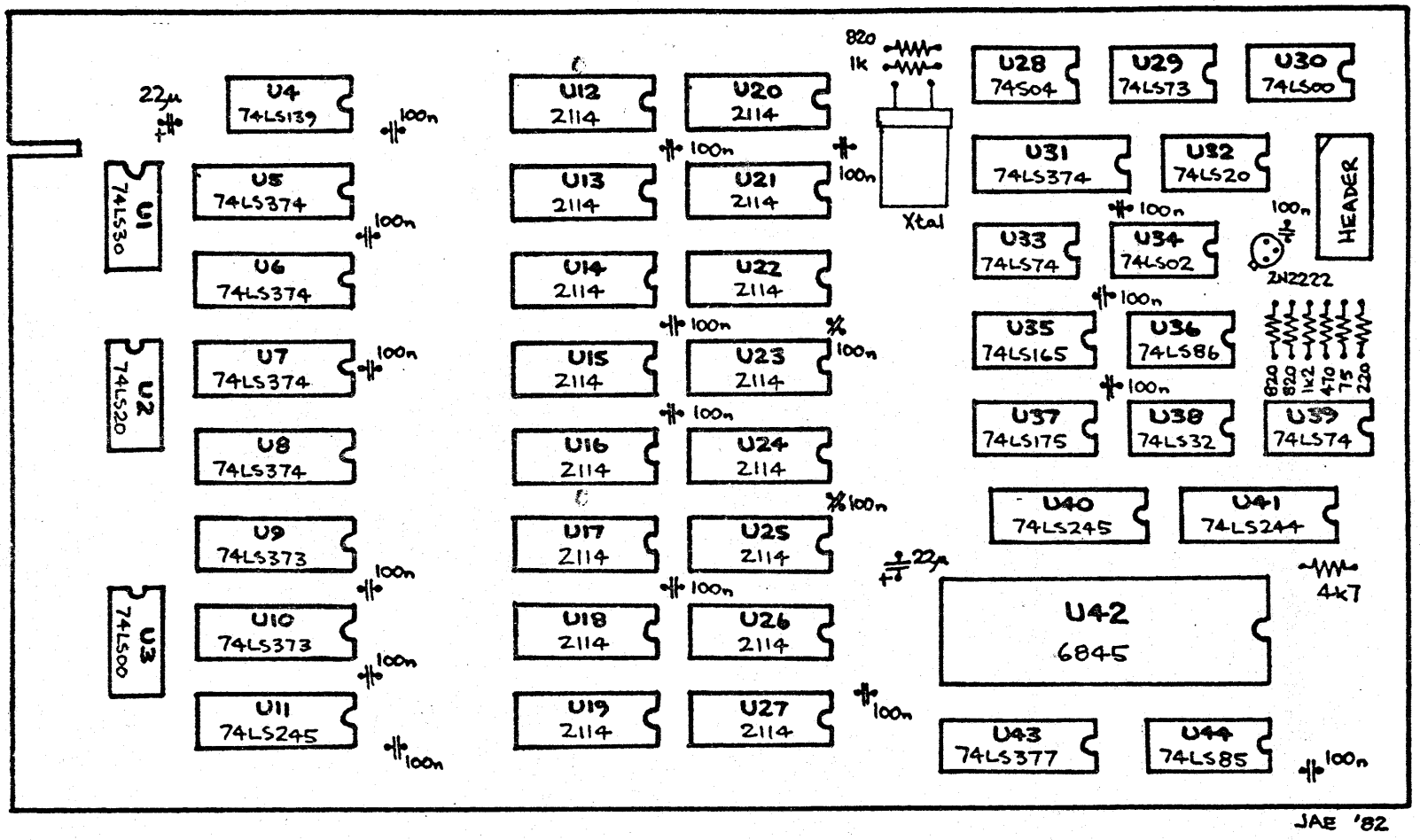
1	75R
1	220R
1	470R
3	820R
1	1k
1	1k2
1	4k7

Capacitors

2	22u tantalum
19	100n ceramic

Miscellaneous

1	14,1926 MHz crystal
1	2N2222 transistor
12	14 pin IC sockets
5	16 pin " "
16	18 pin " "
11	20 pin " "
1	40 pin " "
1	16 pin IC header



COMPONENT OVERLAY

C3-BUS FLOPPY DISC CONTROLLER

Jonathan Eva

Introduction

The C3Bus floppy disc controller is designed to interface up to four 5-1/4" (minifloppy) disc drives to the C3Bus. The card can support single or doubled sided drives and is capable of supporting single or double density recording techniques. Side and density selection are accomplished by software. In addition, the card performs the memory bus to I/O bus transformation required by the fully expanded (256K byte addressing) C3Bus.

Circuit Description

The circuit may be split up into four parts:

i) Address decoding and card selection,
ii) Data buffering and latching,
iii) Floppy disc control,
iv) Floppy disc interface.

These will be dealt with in separate sections.

1. Address decoding and card selection

This circuitry differs depending on whether the bus is connected for 64K or 256K addressing.

64K: In this case, address lines A4 to A7 and control lines VMA and IOS are decoded by U1, U2 and U8a, in conjunction with DIL switches A-1 to A-6, to produce the Card Select signal. U3, U4 and DIL switches B are not included in the circuit.

Note that switch A-5 must be closed and A-6 must be open in this configuration. The settings for DIL switches A-1 to A-4 are given in table I.

256K: In this case, the full 18 bit address bus is decoded by U1, U2, U3 and U4 in conjunction with DIL switches B-1 to B-8 and A-1 to A-6. Switches B-1 to B-8, A-5 and A-6 decode address lines A17 to A8 to select the 256-byte IO block address within the 256K memory map and thus produce the new IOS signal for the IO bus. Switches A-1 to A-4 decode address lines A4 to A7 to select the card address within the IO block as normal. The new IOS signal is linked via link "A" to pin 24 of the bus.
The settings for switches B-1 to B-8, A-5 and A-6 are described in table II. The settings for switches A-1 to A-4 are again given in table I.

A-1	A-2	A-3	A-4	Hex Address
Ø	Ø	Ø	Ø	Ø4 - ØB
Ø	Ø	Ø	1	14 - 1B
Ø	Ø	1	Ø	24 - 2B
Ø	Ø	1	1	34 - 3B
Ø	1	Ø	Ø	44 - 4B
Ø	1	Ø	1	54 - 5B
Ø	1	1	Ø	64 - 6B
Ø	1	1	1	74 - 7B
1	Ø	Ø	Ø	84 - 8B
1	Ø	Ø	1	94 - 9B
1	Ø	1	Ø	A4 - AB
1	Ø	1	1	B4 - BB
1	1	Ø	Ø	C4 - CB
1	1	Ø	1	D4 - DB
1	1	1	Ø	E4 - EB
1	1	1	1	F4 - FB

TABLE I : CARD ADDRESSING
Note : 1 = switch ON, Ø = switch OFF

A-5	A-6	B-1	B-2	B-3	B-4	B-5	B-6	B-7	B-8	IO Block Address
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	ØØØØØ - ØØØFF
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	ØØ1ØØ - ØØ1FF
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	ØØ2ØØ - ØØ2FF
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1	ØØ3ØØ - ØØ3FF
		•					•			•
		•					•			•
Ø	1	1	1	1	1	1	1	1	Ø	1FEØØ - 1FEFF
Ø	1	1	1	1	1	1	1	1	1	1FFØØ - 1FFFF
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	2ØØØØ - 2ØØFF
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	2Ø1ØØ - 2Ø1FF
		•					•			•
		•					•			•
1	1	1	1	1	1	1	1	Ø	Ø	3FCØØ - 3FCFF
1	1	1	1	1	1	1	1	Ø	1	3FDØØ - 3FDFF
1	1	1	1	1	1	1	1	1	Ø	3FEØØ - 3FEFF
1	1	1	1	1	1	1	1	1	1	3FFØØ - 3FFFF

TABLE II : IO BLOCK DECODING IN 256K SYSTEM
Note : 1 = switch ON, Ø = switch OFF

In both 64K and 256K cases, the Card Select signal is used to enable a 2-4 line decoder (U7a) which decodes address lines A2 and A3 to produce the Chip Select signals for the 1793 controller chip (U11) and the Drive/Density/Side Select latches (U9). A0 and A1 are buffered by U6 together with the control signals RDS, WDS and Reset and fed directly to the controller U11.

Note that since A0 and A1 play no part in the address decoding, the latches U9 fold back and occupy four consecutive memory locations. The order of the various registers in the decoded 8 byte block is thus:

0 - Drive/Density/Side select register
1 - Drive/Density/Side select register
2 - Drive/Density/Side select register
3 - Drive/Density/Side select register
4 - FDC Command/Status register
5 - FDC Track register
6 - FDC Sector register
7 - FDC Data register

2. Data buffering and latching

The two Chip Select signals from U7 are gated together with RDS and WDS by U8b, c and d to produce the Enable signal for the data buffers U5. This signal also provides the trigger for the Motor On monostable (U16), which means that the floppy disc drive motors turn on automatically when the controller card is accessed and remain on until a fixed period of inactivity has elapsed (approximately 15 seconds).

The buffered data lines are fed to the controller U11 and the selection latches U9. The data is latched into U9 on the rising edge of the WDS strobe.

Four data bits are latched into U9. These are D0, D1, D6 and D7 and have the following significance:

D0, D1 - These are the binary encoded Drive Selection lines (D0 being the LSB) and are decoded into four individual drive select lines by U7b, wich is enabled via the HLD signal from the controller.

D6 - This is the Side Selection line which goes directly to the drive interfacing.

D7 - This is the Density Selection line, which is inverted by U10 to provide the DDEN control line for the controller circuitry.

3. Floppy disc control

The actual disc control section is considerably simplified by the use of the Western Digital three-chip set, comprising the main controller chip (U11), the floppy support logic (U12) and the four-phase clock generator (U13). The circuit configuration used is basically that supplied in the WD data sheets.

Interrupt signals DRQ and INTR are buffered and inverted by U1 and U2 and fed to bus lines IRQ and NMI via DIL switches A-8 and A-7.

The 1 MHz clock signal for U11 is derived from a 4 MHz crystal oscillator built around three inverters (U10). The 4 MHz output signal is divided down by U15 to produce the required 1 MHz square wave.

The VCO used in the circuit (U14) is a 74LS124 - this chip has been used in preference to the 74S124 or 74LS629 specified by Western Digital. If either of these two chips is used the 47pF frequency control capacitor will need to be increased to 82pF.

Three preset variable resistors are used to set the controller circuitry up - the adjustment of these is covered in a later section.

Monostable U21 provides the required delays after motor startup and drive head load (0,6 sec and 50 msec respectively) before disc read/write activity begins. The two sections of U21 are triggered by the rising edges of the Motor On and Head Load (HLD) signals. The outputs are ANDed by part of U17 to produce the HLT (Head Load Timing) signal which is fed back to the controller.

4. Floppy disc interfacing

The outgoing signals to the disc drives are buffered by non-inverting open-collector (U17) or inverting open-collector (U18) buffers (as appropriate) before being fed to the disc drives. The Side Select signal (interface pin 32) is isolated from the disc interface by link "B" to permit the easy use of single-sided drives.

Incoming signals are terminated by 220/330 ohm resistor networks and (effectively) non-inverting Schmitt trigger buffers to provide maximum noise immunity. The Read Data signal is processed by U16b to ensure that all read data pulses are the correct width (250ns - 500ns) before being fed to the controller and data separator circuitry.

Construction

Construction is fairly straightforward. As usual, the component overlay is actual size to allow easy location of component holes.

If the board is to be used in a 64K system, components U3, U4, DIL switches B and eight 4k7 resistors may be omitted if

desired. It is recommended, however, that the resistors and switches be soldered in and sockets provided for U3 and U4 to allow painless expansion in the future. For a similar reason it is recommended that sockets be soldered in positions "Header A" and "Header B" even if an edge connector is going to be used.

Links "A" and "B" can be inserted - "A" for a 256K sytem, "B" for double sided drives.

Either a 34-way edge connector or two 16-pin header plugs may be used to connect the drives to the card. The edge connector corresponds identically to the connector on the disc drives themselves, while the pin connections for the headers are given on the circuit schematic. Note that it will be necessary to remove the last two lines (33 and 34) from the cable if the header plugs are used to connect to the card. These are normally unused lines.

Setting up

This is a fairly difficult procedure to accomplish without adequate equipment, and it is recommended that, if necessary, you enlist the help of somebody who has a good high-frequency oscilloscope (or even better, a logic analyser), a frequency counter and a high impedance voltmeter.

Ensure that all presets P1, P2 and P3 are set to mid-position, and remove the controller chip U11 and the floppy support logic U12. The disc drive must be disconnected from the card.

Apply power to the board. If you are using separate supplies for the +12V and +5V (i.e. two individual supplies) then ensure that the +12V is always the first to be switched on and the last to be switched off. If your supplies are turned on and off by a common switch then this will not be a problem.

Check that a 1 MHz square wave is present on pin 8 of U15.

Link pin 24 of U11's socket to pin 5 of U12's socket by a small piece of wire. Check the signal present on pins 1, 3, 5 and 7 of U13. Each pin should have a narrow negative-going (+5 to Ø) pulse occurring every microsecond on it. Adjust P1 to make these pulses 125ns wide.

Switch the power off, and insert U12.

Switch the power on and measure the voltage on pin 2 of U14 (the VCO). Adjust P2 until the voltage measures 1,4V. Note: be careful to use a high-impedance voltmeter for this measurement!

Attach a frequency meter to pin 7 of U14 and adjust P3 until the meter reads 2 MHz exactly. If you are not using a 74LS124 (or have one that is out of spec) it may be necessary to change the value of the 47pF capacitor to achieve this.

This completes the setting-up procedure. Turn the power off and replace U11. The board is now ready for use.

COMPONENTS LIST

Integrated circuits

2	74LS136	O-C EXOR gates
*2	74LS136	O-C EXOR gates
1	74LS245	Bidirectional buffers
1	74LS367	Buffers
1	74LS139	Dual 2-4 decoder
1	74LS00	NAND gates
1	74LS377	Octal D flip-flops
1	74LS04	Inverters
1	WD1793	FDC (may also use WD1797)
1	WD1691	Support logic
1	WD2143	Clock generator
1	74LS124	VCO
1	74LS93	4-bit counter
2	74LS123	Dual monostables
1	7407	O-C buffers
1	7406	O-C inverters
2	74LS14	Schmitt inverters

Resistors

1	68R	1/4 watt	1	33k	1/4 watt
4	220R	" "	2	47k	" "
4	330R	" "	1	150k	" "
1	820R	" "	1	390k	" "
4	1k	" "			
1	2k7	" "			
6	4k7	" "	1	4k7	single-turn preset
*8	4k7	" "	1	22k	" "
2	10k	" "	1	100k	" "

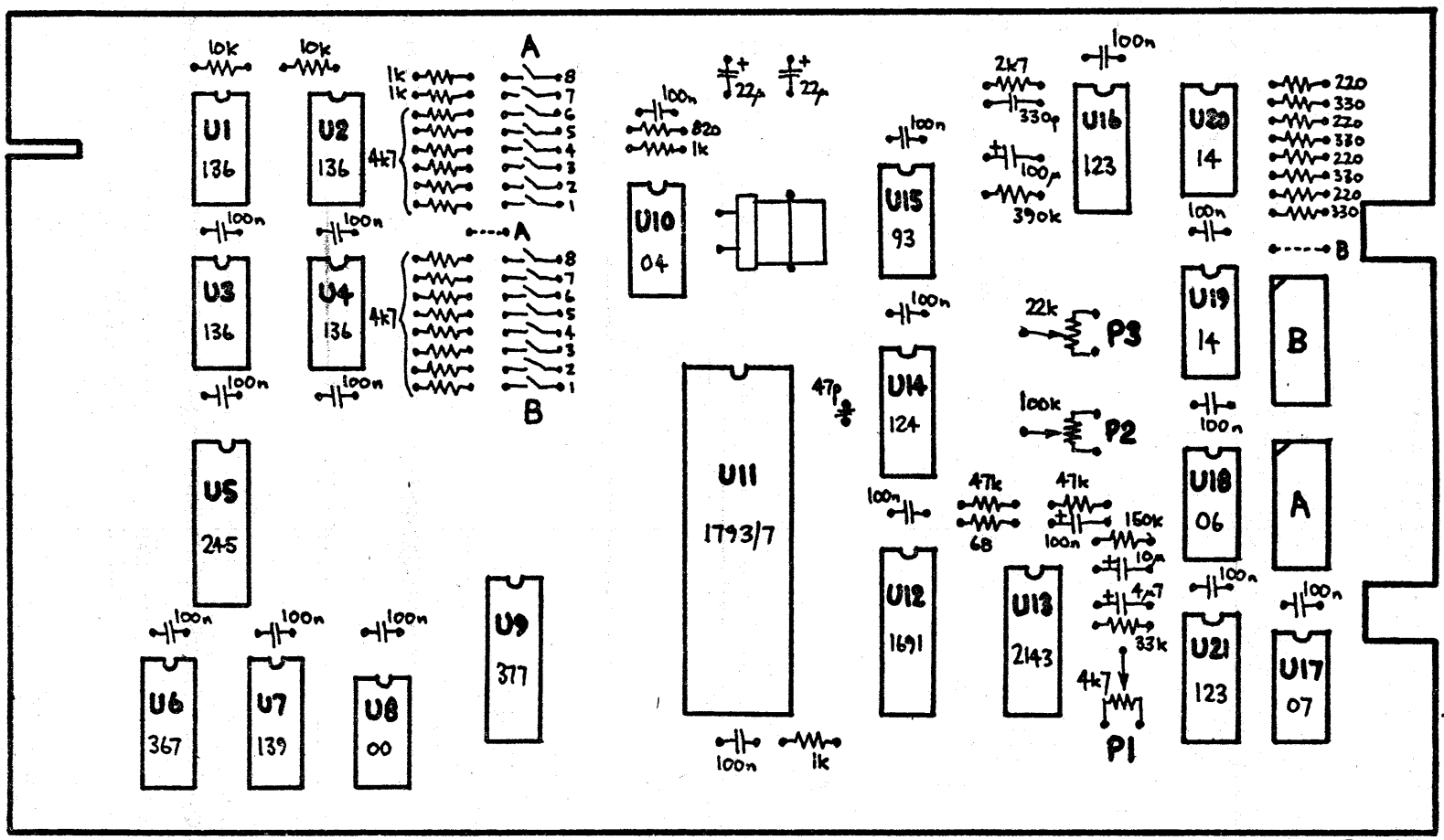
Capacitors

1	680n	tantalum	1	47p	ceramic
1	4u7	"	1	330p	"
1	10u	"	17	100n	"
2	22u	"			
1	100u	"			

Miscellaneous

9	14-pin	IC sockets	1	4 MHz	crystal
*2	14-pin	" "	1	8-way	DIL switch
7	16-pin	" "	*1	8-way	DIL switch
1	18-pin	" "			
3	20-pin	" "			
1	40-pin	" "			

Note: Quantities marked with a * are required for 256K systems only.



COMPONENT OVERLAY

C3Bus to 256K Addressing

Jonathan Eva

Introduction

The original C3Bus allows only 16 lines for memory addressing, thus enabling up to 64K of memory to be directly addressed. In many situations it is desirable to be able to directly address much more memory (e.g. to implement pseudo-disk storage, to allow multi-tasking etc.) and to enable this to occur, the C3Bus has been modified.

When making the modification, it must be remembered that existing cards must continue to operate properly on the bus with little or no modification. It is thus not possible to make radical timing changes to any signals or to remove signals which might be used by existing cards.

Inspection of the C3Bus shows that only two signals have the same timing as the existing 16 address lines, these being VMA and IOS. Of these two signals, VMA is generated only by 6800 based systems, but is used in the address decoding of existing I/O cards, and IOS is obviously used by all I/O cards. It is thus apparent that if these two signals are used as extra address lines, they must be restored in some fashion for use by the existing C3Bus cards.

Description of the modification

Bearing the above in mind, the modification is as follows:

The C3Bus is divided into two sections - the "memory" bus and the "IO" bus. The memory bus contains a full 18-bit address bus with no IOS or VMA signals, while the IO bus is identical to the original C3Bus and accepts existing C3Bus cards.

The interface between the IO bus and the memory bus is performed by the Floppy Disk Controller (FDC) card. This card accepts the 18-bit address bus and decodes a 256-byte block to regenerate the IOS signal. VMA is also recreated at this point.

The 6809 CPU card and the Dynamic RAM (DRAM) card occupy the memory bus, and the CRTC, Serial and Parallel cards occupy the IO bus. This is illustrated diagrammatically in figure 1.

Any standard C3Bus card may be plugged into the IO bus. Those cards that need 18-bit addresses and do not require IOS or VMA may be plugged into the memory bus.

Note that the position of two cards in the system is fixed. The FDC card, because it performs the memory to IO bus transformation, cannot be moved, and the DRAM card must occupy its own slot as special modifications are made to it.

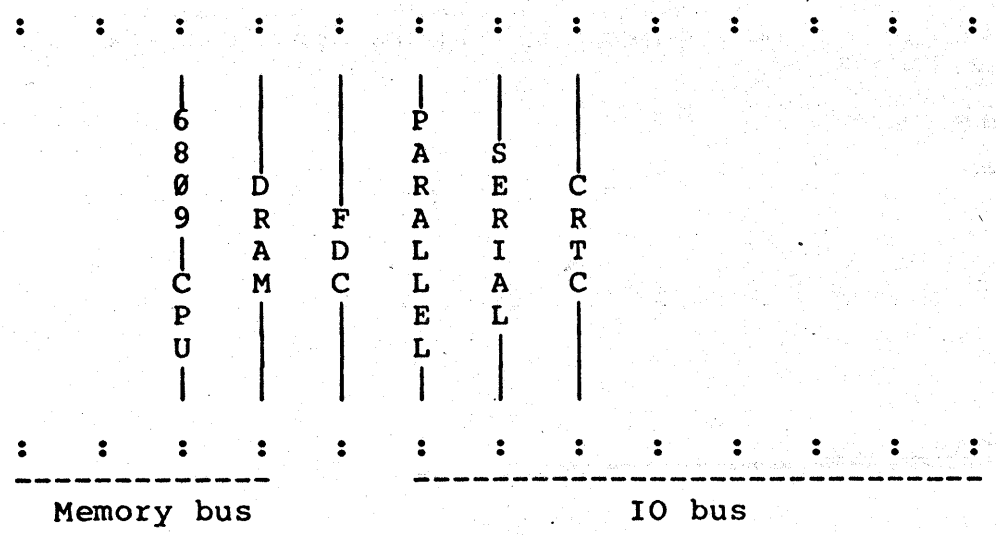


Figure 1. 256K C3Bus structure

Physical modifications

In order to implement the above conversion, it is necessary to make modifications in four places:

i) The bus itself;
ii) The 6809 CPU card;
iii) The Dynamic RAM card;
iv) The FDC card.

These will be dealt with in turn.

1. Modifications to the bus

The modifications required to the bus involve changing three bus lines, and are shown in the attached diagram. These mods are explained as follows:

Because there are no unused lines on the bus, it is necessary to 'borrow' one for the conversion. As neither the DRAM nor FDC boards use WAIT, this is the line chosen.

The FDC board accepts the 18-bit address A0-A17 and decodes a new IOS signal from it. This appears on the WAIT pin and is taken to the IO bus IOS line, and to the DRAM board so that the memory may be disabled when an IO access is occurring (this is why the position of the DRAM board is fixed in the memory bus.) The WAIT line on the IO bus skips over the DRAM and FDC boards, and is reconnected to the memory bus.

The VMA line is passively pulled high, since during a 6809 VMA cycle the address bus is set to $FFFF and no illegal accesses will occur.

2. 6809 CPU card modifications

DIL switches C must be set as follows:

Switches 1, 2 : switch ON
3, 4, 5, 6, 7, 8 : switch OFF

Another modification is necessary to correct a design fault in the CPU card. The modification is:

i) Remove the pullup resistors on the outputs of U4. (These are the two lowest 3k3 resistors of the six between U3 and U5, i.e. the two closest to DIL switches C.)

ii) Remove the inverters from the outputs of U4 as follows:

1. Remove U1Ø (74LSØ4) from its socket, and isolate pins 1Ø and 12 by bending them up or breaking them off. Re-insert U1Ø into its socket.
2. Short pins 1Ø and 11 of U1Ø on the solder side of the board.
3. Short pins 12 and 13 of U1Ø on the solder side of the board, taking care not to touch the track passing between them.

3. Dynamic RAM card modifications

These are the most extensive modifications. They are performed as follows:

i) Viewing the board from the solder side, locate the seven shorting pads and four linked pads (shown diagrammatically in the attached figure). Break the four linked pads with a sharp knife, taking care not to damage any other tracks, and connect all the shorting pads with a small blob of solder except the one in the lower left corner under U5 (refer to figure). This must be left open.

ii) With small solder blobs, short the +5V, -5V and +12V bus connectors together close to the bus (refer to figure). Cut or remove the -5V and +12V bus contacts so that the board no longer connects to the -5V and +12V bus power rails. This converts the +12V supply to the RAMs (pin 8 on the 4116) to +5V, and ties the -5V supply (pin 1 on the 4116) to +5V so that 64K RAMs with internal refresh will operate correctly.

iii) Cut the +5V power rail on the solder side of the board just next to the upper left shorting pad (refer to figure). This converts the old +5V power supply (pin 9 on the 4116) to the extra address line A7.

iv) Link the WAIT contact on the bus (pin 24 - not connected) to pin 3 of U4 (74LS138) with a thin piece of wire on the solder side of the board. This links the new IOS signal from the FDC into the decoding, so that the RAM is disabled for IO accesses.

v) Remove the middle one of the three 1ØuF tantalum capacitors next to the RAM array. This capacitor was connected to the -5V supply line, which has now been tied to +5V.

The RAM chips may now be replaced with 4164 64K x 1 types, of similar speed or faster. Either internal refresh or standard (pin 1 non-connected) types may be used. The board is now

configured for 256K operation.

4. FDC card modifications

Modifications to the FDC card simply entail installing ICs U3 and U4, and DIL switches B. Insert link "A" (located between DIL switches A and B) and set the switches to the following positions:

```
Switch A: 4, 5, 6       : switch ON
          1, 2, 3, 7, 8 : switch OFF
Switch B: 1, 2, 3       : switch ON
          4, 5, 6, 7, 8 : switch OFF
```

The IO page is now located at physical addresses 3E000 - 3E0FF.

Documentation Changes

The latest documentation (released January 1984) has all corrections made for the 256K mod. If you do not have this documentation, contact the 6809 Group leader for a copy.

Populating the RAM card

When populating the RAM card, it is important to bear in mind that the most significant bank (U12 - U19) must be present if the software is to function correctly.

The reason for this is that the monitor, on reset, searches through all 256K looking for memory so that it can set up the Dynamic Address Translation memory on the CPU board. Because the IO page is at physical address $E000 - $E0FF in the 64K system, and $3E000 - $3E0FF in the 256K system, the monitor must make the logical IO page correspond to the physical IO page and thus simply sets up the DAT RAM so that this mapping takes place. It also uses logical block $E100 - $EFFF for the screen, system stacks and monitor scratchpad... so if this RAM is not present, nothing will work.

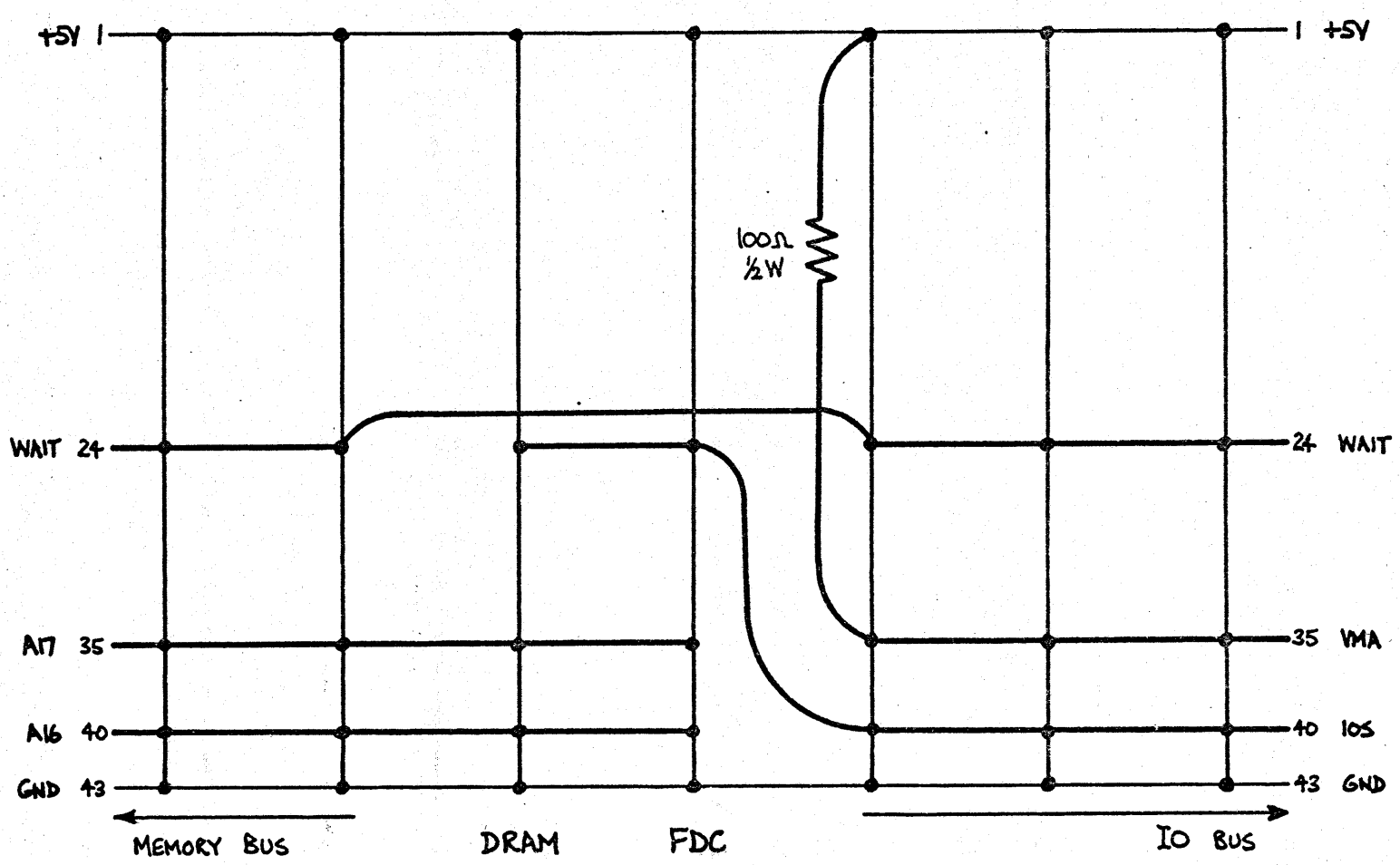
The other three blocks on the RAM card (U20 - U43) can be filled in any order. The monitor will automatically determine whether they are present and will allocate them appropriately.

Note that this only applies to the 6809 Microsystem Monitor V4.0 and later. Monitors of version 3.7 or earlier will not perform address translation correctly - for these monitors, it is necessary to install U36 - U43 and U12 - U19, the other two banks not being used.

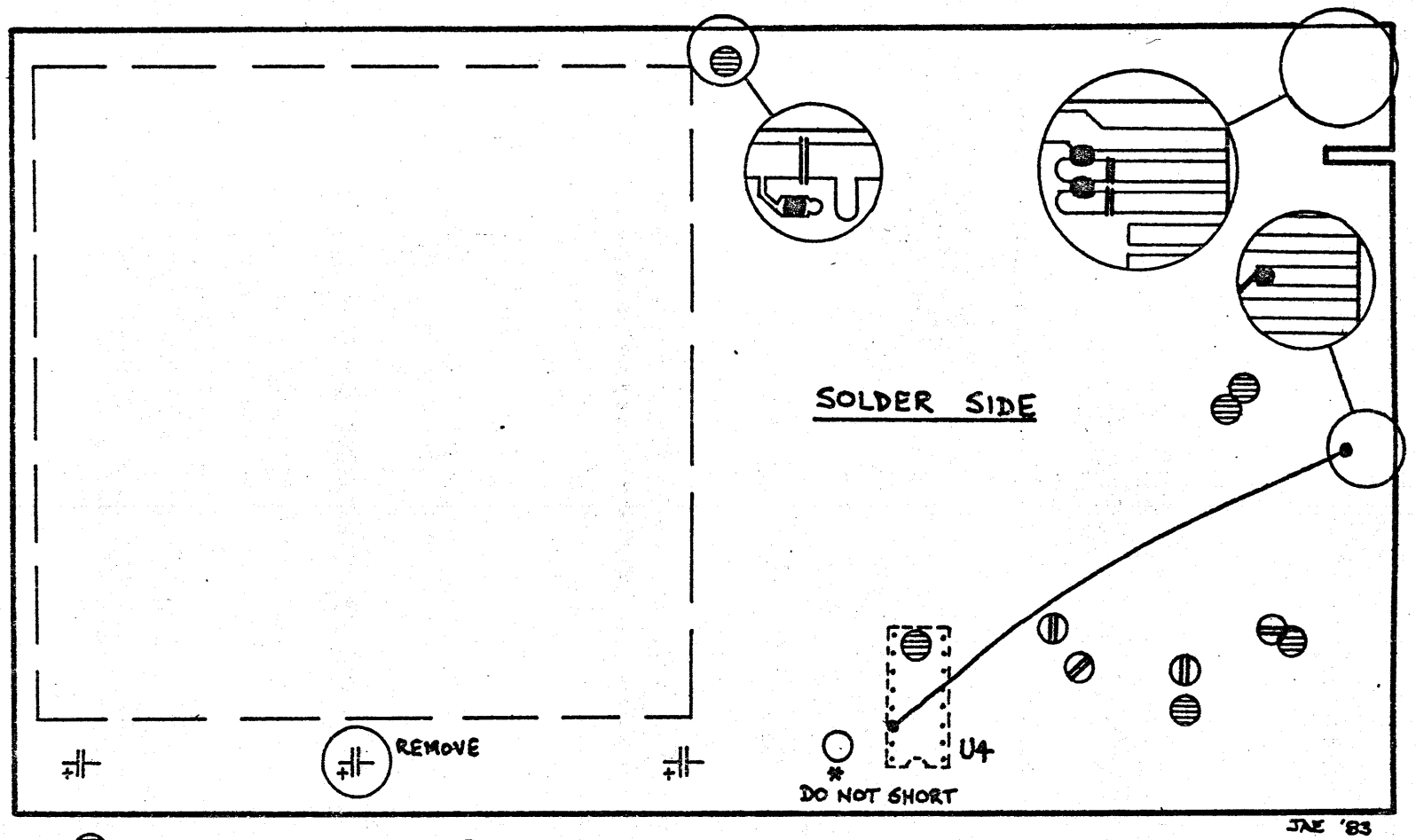
Conclusion

This completes the modification. The cards may now be plugged into the correct bus positions as illustrated in Figure 1 above. Note that the -5V power supply is not used on any boards, while the -12V supply is only used on the Serial board. These two supplies may be removed if desired, but they may be used on future boards.

If the system does not function on switch on, recheck all modifications made, especially the DRAM and CPU boards, where accidental solder splashes or track breaks are possible. Recheck all DIL switch settings, preferably against the original board documentation as a double check, watching for accidental changing of switches not involved in the modification. If these checks do not bring success, more extensive testing of the system will have to be employed.

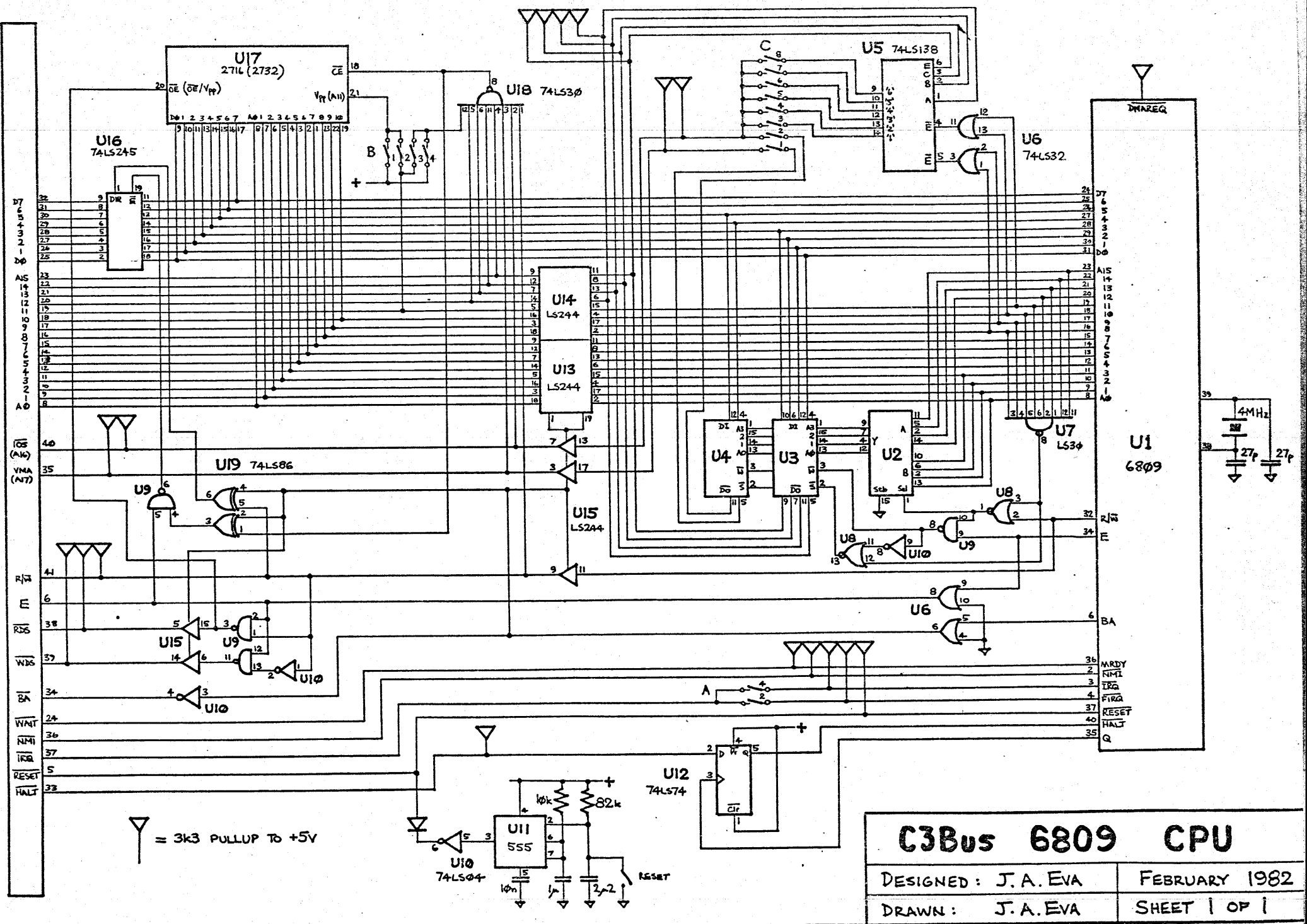


C3BUS 256K MODIFICATION



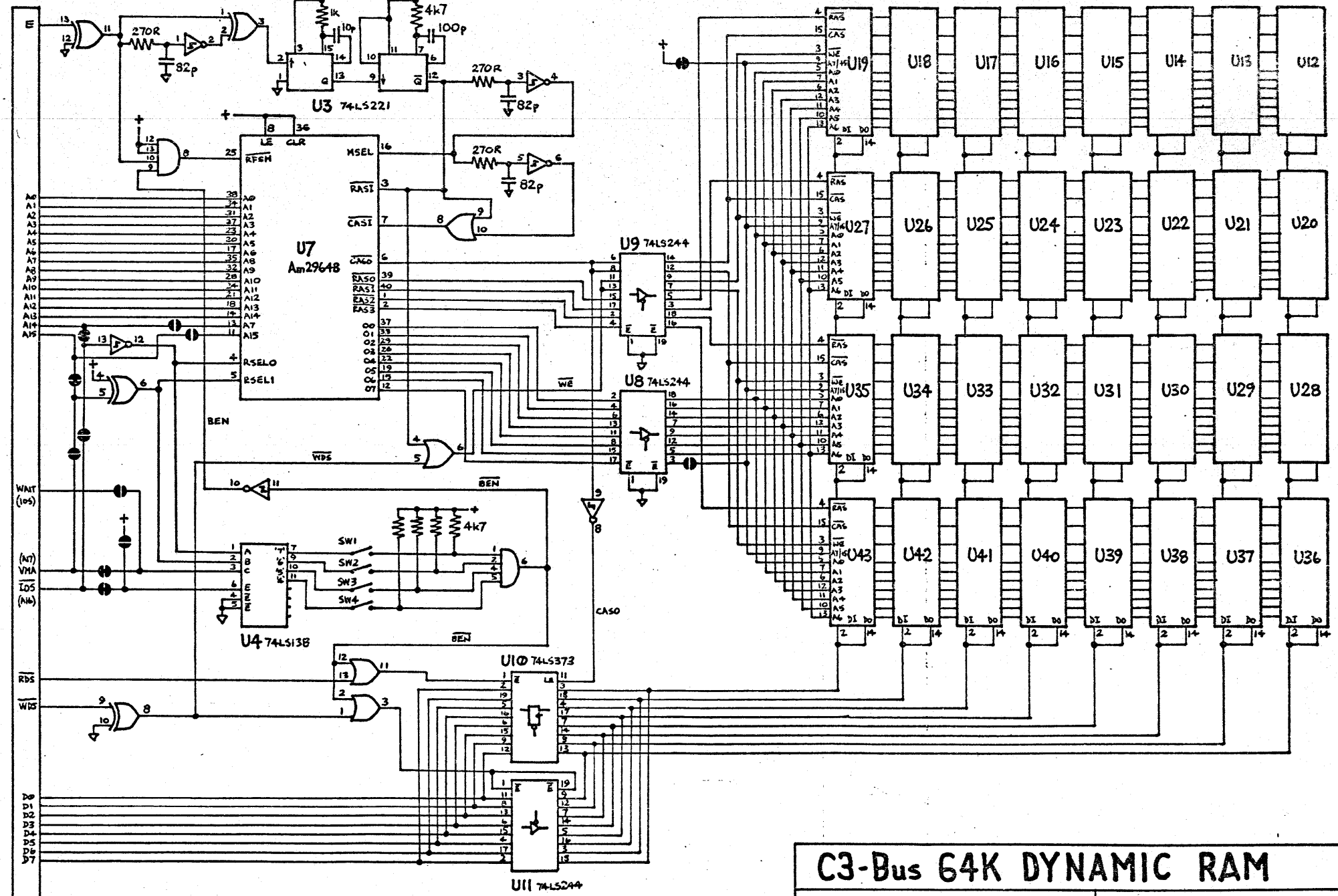
- SHORT PADS TOGETHER - BREAK LINKED PADS

C3BUS DYNAMIC RAM - 256K CONVERSION



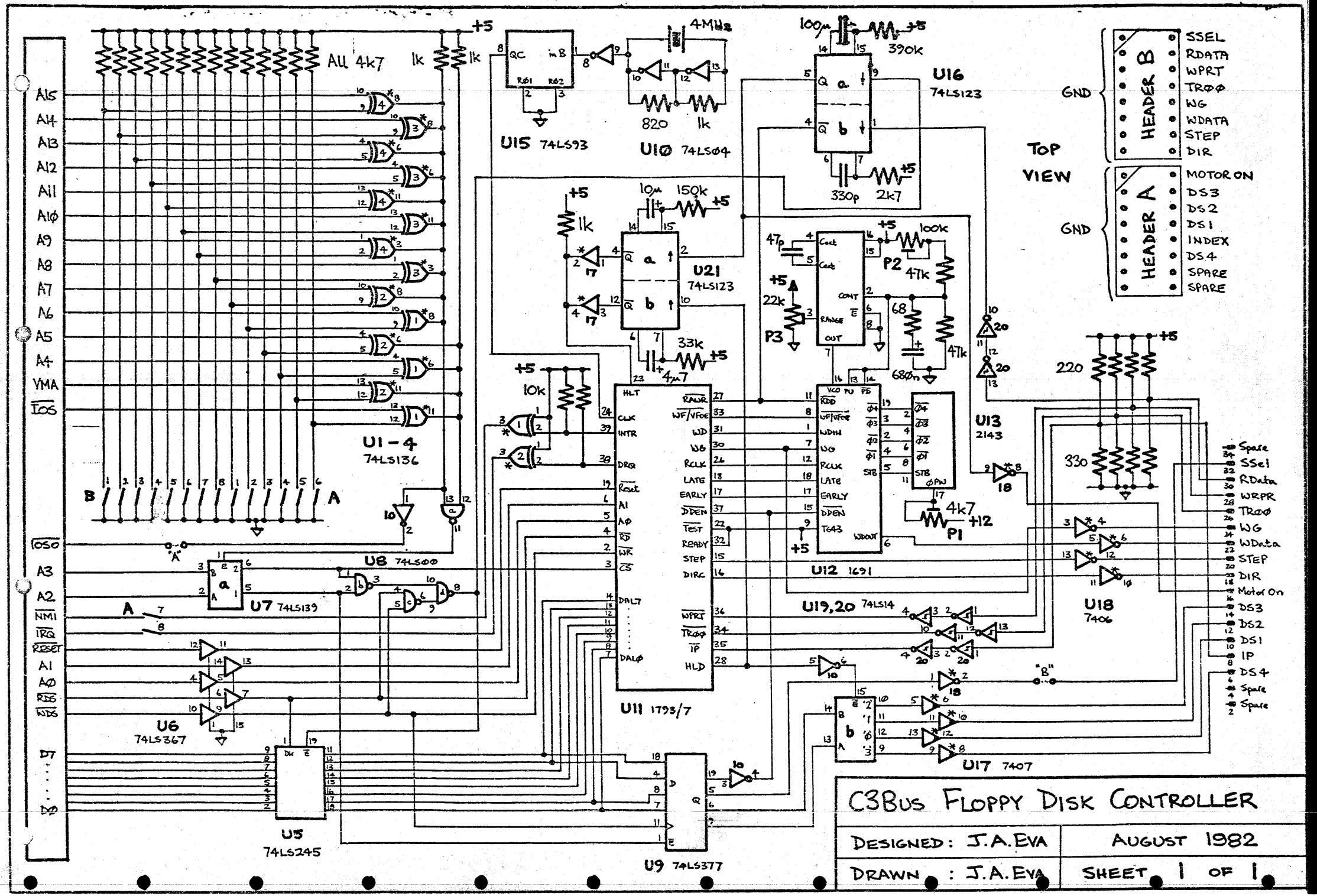
C3Bus 6809 CPU

DESIGNED : J. A. EVA	FEBRUARY 1982
DRAWN : J. A. EVA	SHEET 1 OF 1



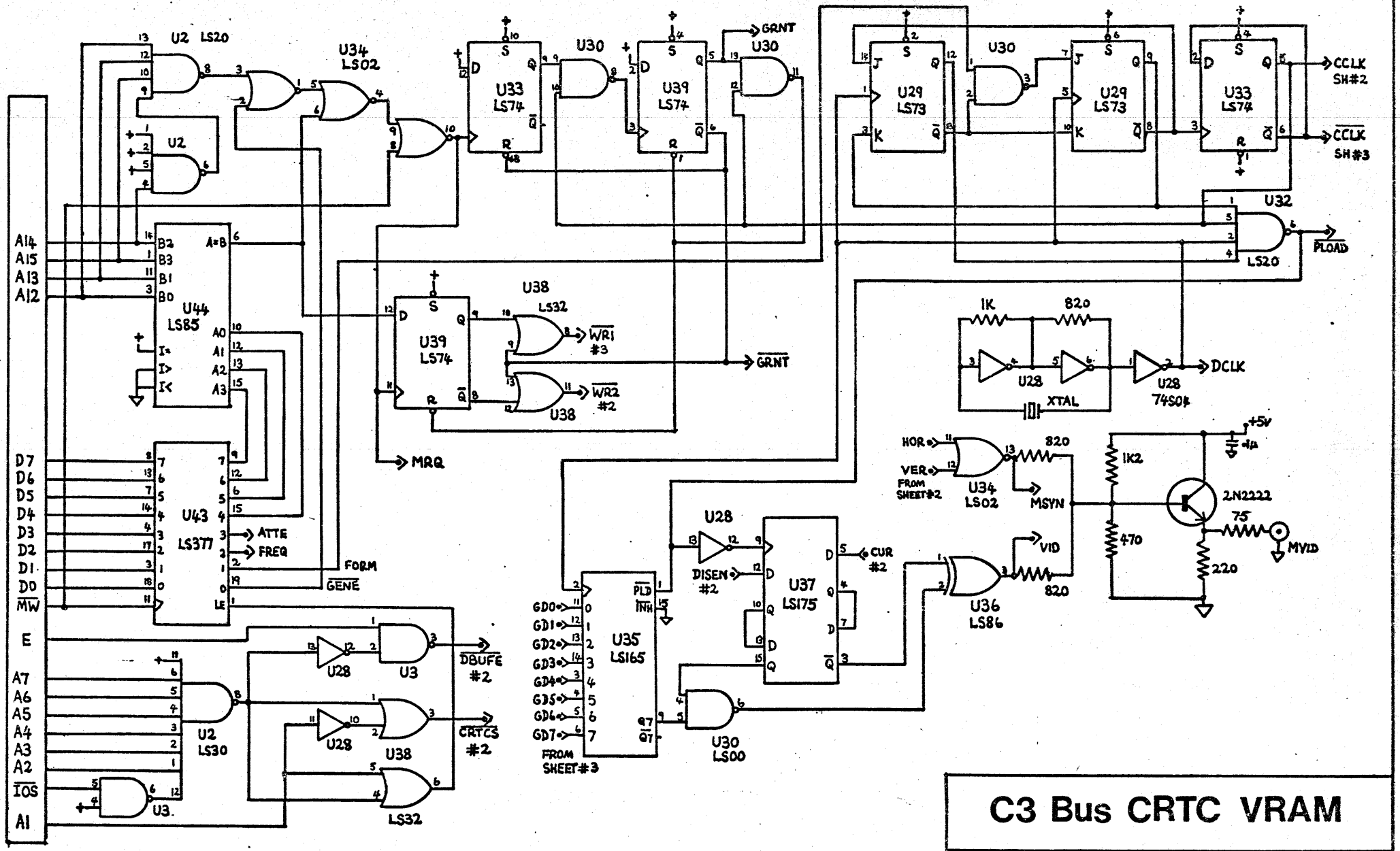
C3-Bus 64K DYNAMIC RAM

DESIGNED : J.A. EVA	SEPTEMBER 1981
DRAWN : J.A. EVA	SHEET 1 OF 1



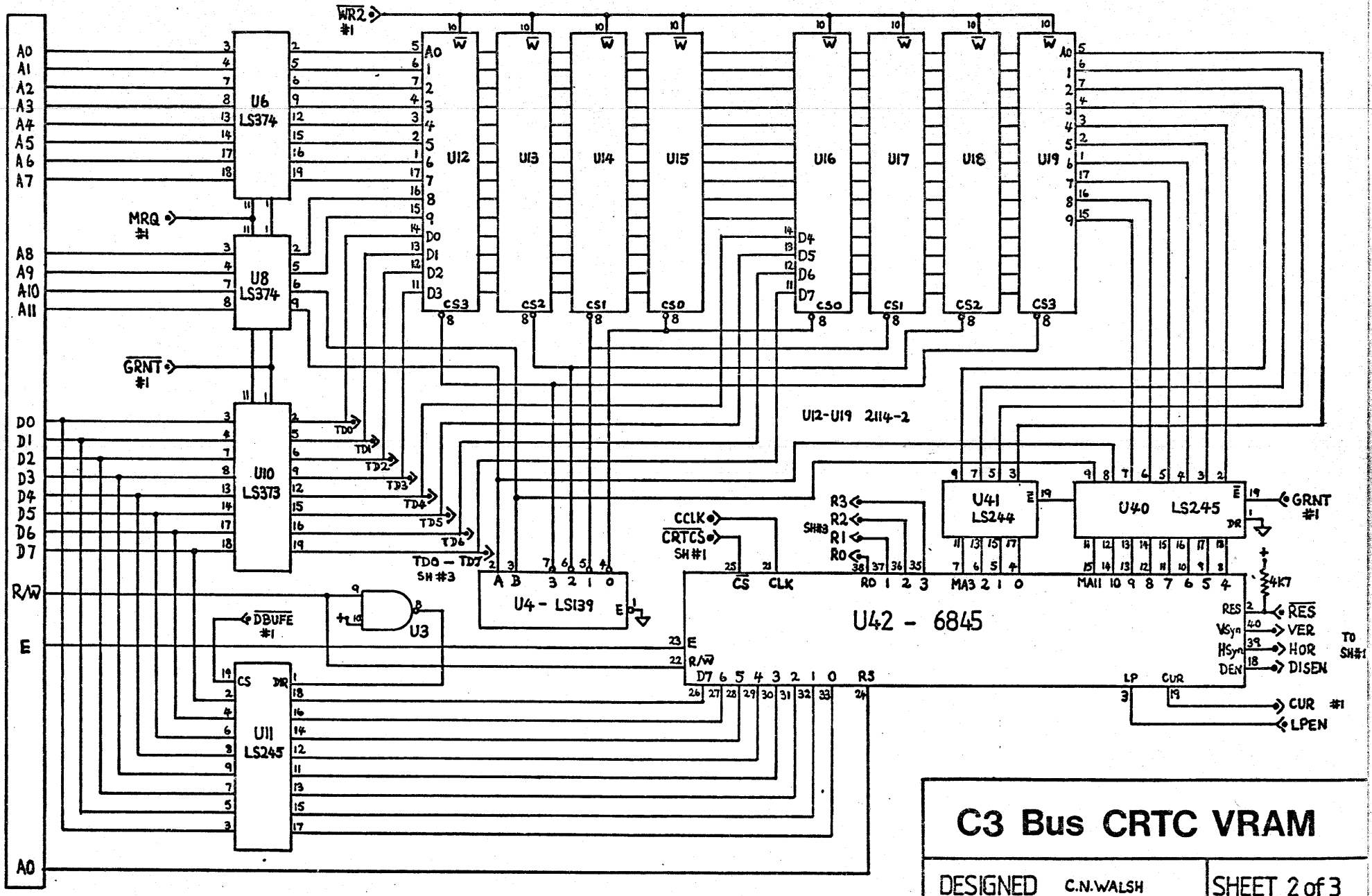
C3Bus Floppy Disk Controller

Designed: J.A.Eva	August 1982
Drawn : J.A.Eva	Sheet 1 of 1



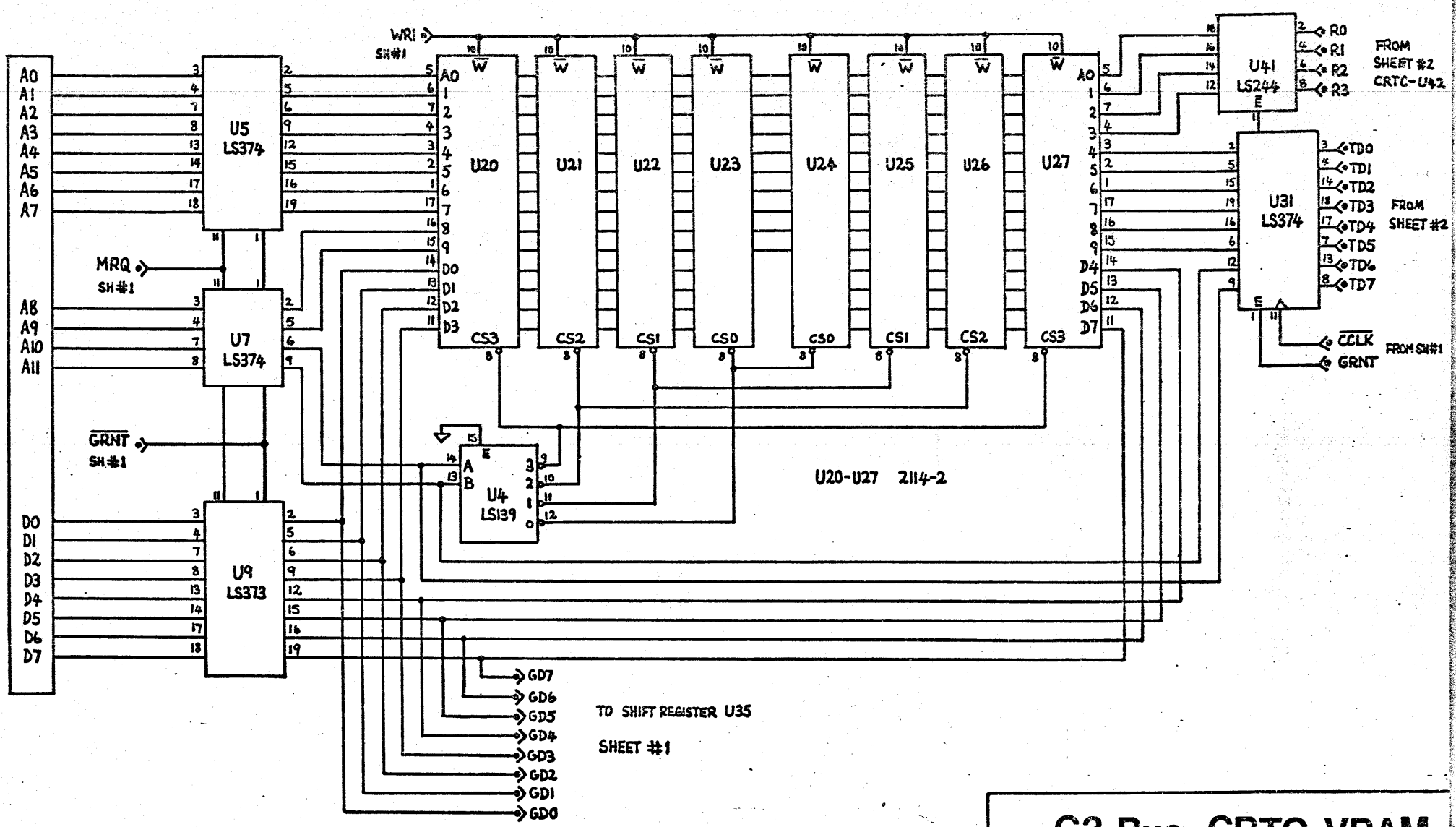
C3 Bus CRTC VRAM

DESIGNED	C.N.WALSH	SHEET 1 of 3
DRAWN	C.N.WALSH	NOV 1982



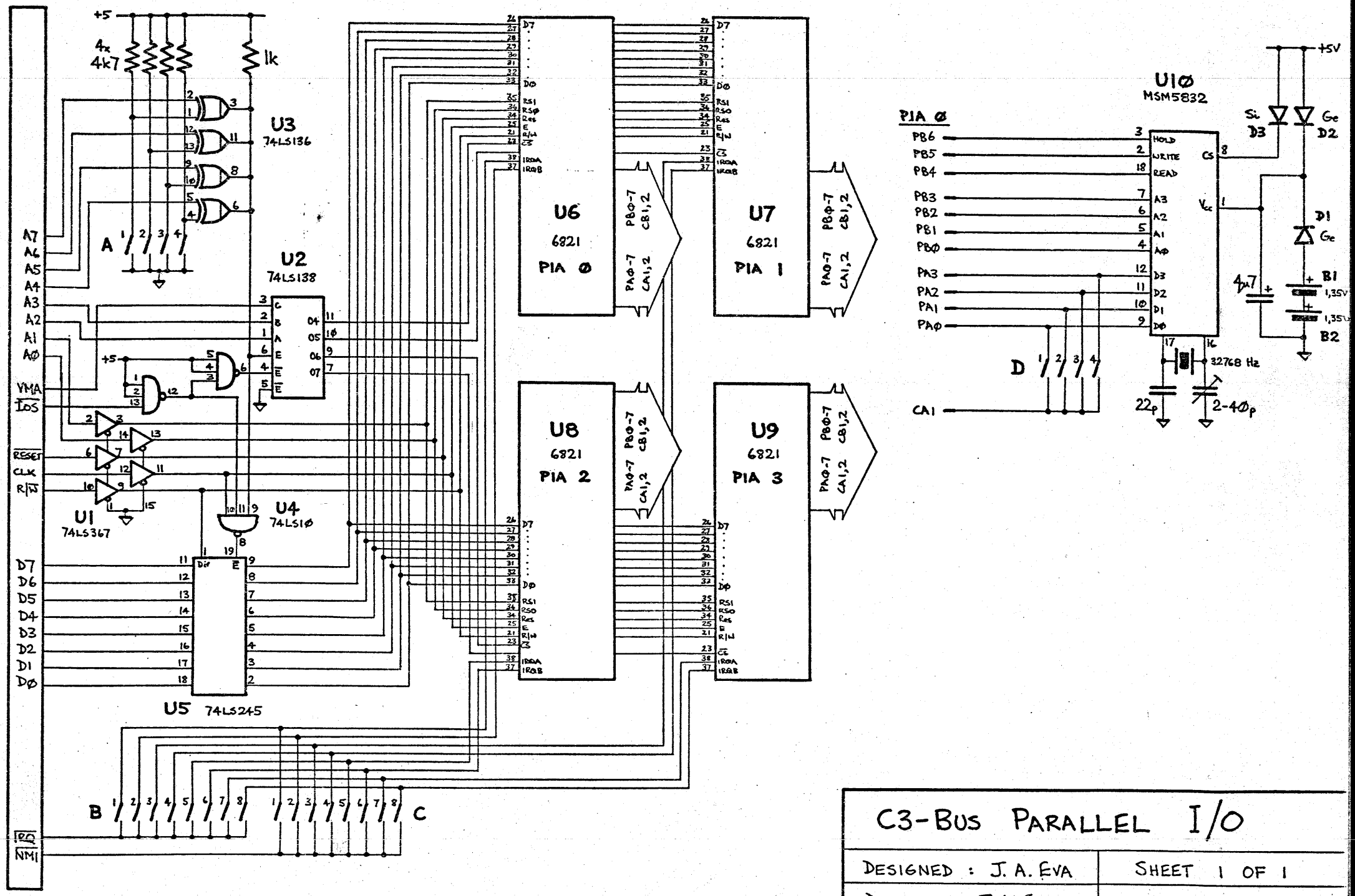
C3 Bus CRTC VRAM

DESIGNED	C.N.WALSH	SHEET 2 of 3
DRAWN	C.N.WALSH	NOV 1982



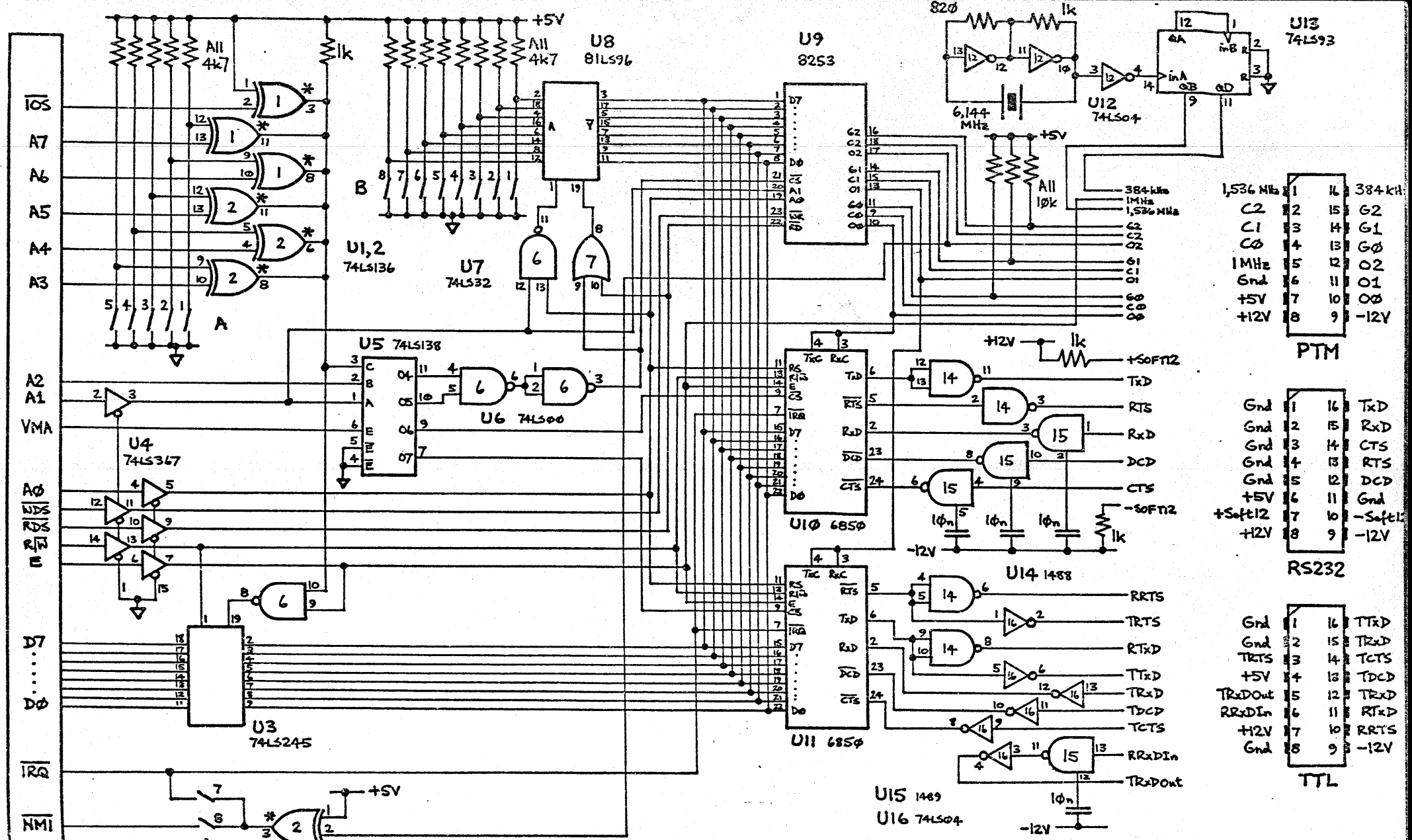
C3 Bus CRTC VRAM

DESIGNED	C.N.WALSH	SHEET 3 of 3
DRAWN	C.N.WALSH	NOV 1982



C3-BUS PARALLEL I/O

DESIGNED : J. A. EVA	SHEET 1 OF 1
DRAWN : J. A. EVA	MAY 1982


IOS
A7
A6
A5
A4
A3
A2
A1
VMA
AØ
WDS
RDS
R/W
E
D7
DØ
IRQ
NMI
All 4k7
1k
+5V
U8 81LS96
U9 8253
U1,2 74LS136
U7 74LS32
U5 74LS138
U6 74LSØØ
U4 74LS367
U3 74LS245
U1Ø 685Ø
U11 685Ø
U14 1488
U15 1489
U16 74LSØ4
U12 74LS04
U13 74LS93
6,144 MHz
82Ø
All 1Øk
384kHz
1MHz
1,536 MHz
G2
G1
GØ
O2
O1
OØ
+12V
-12V
+SOFT12
-SOFT12
TxD
RTS
RxD
DCD
CTS
RRTS
TRTS
RTxD
TTxD
TRxD
TDCD
TCTS
RRxDIn
TRxDOut
1Øn
PTM
RS232
TTL
C3BUS SERIAL I/O CARD
OCTOBER 1982
DESIGN: A.M.STALLKAMP, J.A.EVA
SHEET 1 OF 1
DRAWN: J.A.EVA