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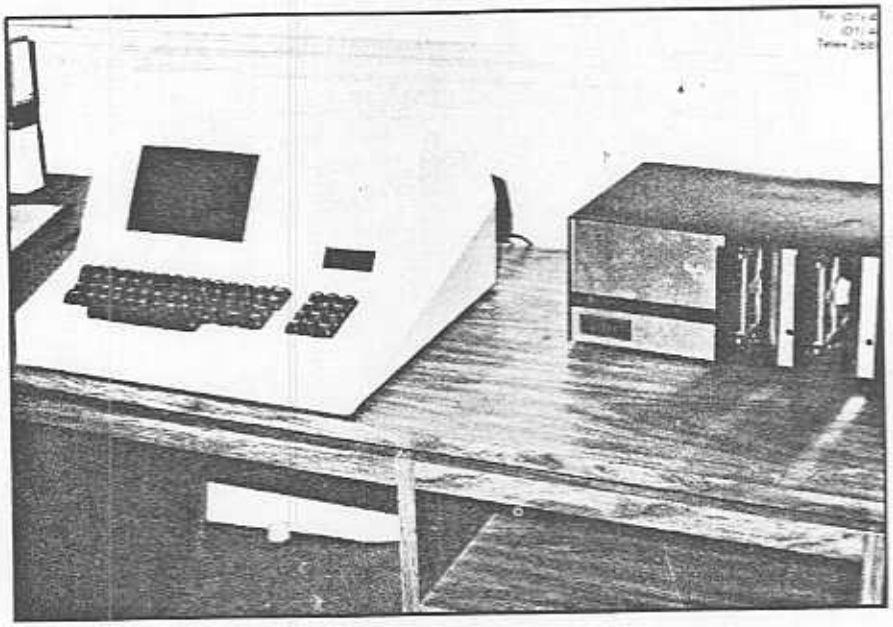
The 6809 microprocessor looks like reviving interest in the S50 bus. We take a look at its various virtues.

The S100 bus standard has become so accepted by the microcomputer community that other bus standards have tended to be ignored. The S100, with so many manufacturers supporting so many different computers and plug-in cards, has tended to kill off any attempts at alternatives. Perhaps the one exception has been the similarly named S50 bus. In the same way that the S100 came from the control line requirements of the Intel 8080, the S50 came from the Motorola 6800. Most of the similarities and differences between the two buses can be seen in Table 1.



Micro History

In the early days of microcomputing the S50 bus was almost as popular as the S100. Indeed, in this country, there was a time when the S50 was by far the most used, mainly due to the pioneering efforts of Computer Workshop importing SWTP equipment. Later the S100 became the most popular bus, for various reasons many different manufacturers produced equipment based on the S100. The Z80 was the most powerful MPU and was only available on the S100 (a brief experiment using the Z80 on the S50 did not catch on). Microsoft produced a range of powerful software for the 8080/Z80, and eventually Digital Research produced CP/M, a rapidly accepted disc operating system.

My own route into microcomputers was via the S50/6800 system and, like many others, I eventually believed that the S100 was better and switched to an S100/Z80 based system. After some time using CP/M, interfacing various bits and pieces of equipment and trying hard to believe what everyone else was still telling me about S100/Z80 systems, I decided to give the S50 another try. My reasons for abandoning the over-complex, hardly standard S100, the arbitrary architecture of the Z80, and the primitive CP/M, will become clearer during the rest of this article.

S50 Revisited

The basic structure of the S50 bus can be seen in Table 2. Nearly all of the

	S100	S50
Produced By	ALTAIR	South West Tech. Products (SWTP)
1st CPU	8080	6800
2nd CPU	Z80	6809
Other CPUs	8085	6502/Z80 (not popular)
I/O	256 undecoded	8 fully decoded 4, 16 registers each
Improvements	IEEE S100	S50C
Manufacturers	Many	Few large companies
Main DOS	CP/M	FLEX
Software	wide range	not much applications software

Table 1. Similarities and differences between S100 and S50 users.

S50 NAME (pins 1 to 50)	DESCRIPTION
D0	eight bi-directional inverted data lines
D1	
D2	
D3	
D4	
D5	
D6	
D7	
A15	16 address lines
to	
A0	
GRD	Ground
GRD	
GRD	
+8V	
+8V	
+8V	
−16V	
−16V	
not used	Location (index) pin
MRST	Manual Reset
NMI	Non Maskable Interrupt
IRQ	Interrupt
UD2	User defined
UD1	User defined
Ø2	Phase two clock (1-2 MHz)
VMA	Valid address indication
R/W	Read/Write
Reset	
BA	Bus available
Ø1	Phase one clock
HALT	
110b	110 baud line
150b	150 baud line
300b	300 baud line
600b	600 baud line
1200b	1200 baud line

Table 2. The S50 bus structure.

BOARD THE S50

Internals of an S50 based machine. The small cards are mounted on the S30 peripheral bus.

bus lines are derived from the 6800 MPU's connections. 16 address lines provide the same amount of addressing as the S100. Eight bi-directional data lines contrast with the S100's 16 unidirectional data lines. Most of the other lines are fairly straightforward and self-explanatory. Anyone familiar with the S100 will be surprised at the relatively few control lines used. That they are enough is something that can only be proved by experience.

The greatest difference between the S50 and the S100 is, in fact, not part of the main bus definition at all. The S50 bus has an auxiliary I/O bus consisting of 30 pins (not strictly a bus at all because not all the pins are paralleled). This is sometimes referred to as the S30 bus and its specifications can be seen in Table 3. The most unusual feature of the S30 bus is the presence of pin 1, an I/O select pin. The S50 bus is so organised that every S30 bus slot occupies a certain number of address locations (usually four, but see the definition of the S50C later) and when an address in the slot's range is output on the main bus the I/O select pin goes low. This means that any I/O card plugged into an S30 slot need only examine pin 1 to discover if it is being addressed or not. Thus, I/O cards need very little circuitry for this purpose.

Although not part of the S50 standard, most S50 computers have eight S30 I/O ports, usually at the rear of the main chassis. As the S50 bus is organised around the 6800 MPU the S30 I/O bus is organised around the 6800's peripheral chips — the 6800 PIA, and the 6850 ACIA. Thus RS0 and RS1 are used as register select lines to determine which control/data register of a 6820 is being addressed. Having only two register selects means that each S30 slot can only access four I/O registers. Thus, more advanced peripheral chips, such as the MOSTEK 6522 VIA, cannot be used. (A problem overcome with the advent of the S50C extended but — see later). To recap, each S30 slot has one I/O select pin which goes low when the slot is addressed and occupies four distinct addresses in the main memory space, usually referred to as an I/O port.

A Simple Interface

To show how easy it is to construct a custom interface on the S50 bus we will consider a simple example. Rather than choosing to interface a standard Motorola device such as a 6820 PIA, which, after all the S30 bus was designed to make easy, we will interface the ZN425E D to A converter chip.

The ZN425E chip is not designed to be used directly on a microprocessor bus and has only eight non-latched data inputs. So, the first thing we must do is to provide a latch. A 74100 octal latch solves this problem nicely and, as we are not too fussy about decoding all of the register locations, a 7402 NOR gate

S30 NAME (pins 1 to 30)	DESCRIPTION
UD3	user defined
UD4	user defined
−12V	
+12V	
GND	
GND	
not used	Location (index) pin
NMI	
IRQ	
RS0	Register select 0
RS1	Register select 1
D0	
D1	
D2	
D3	eight bit bi-directional data lines
D4	
D5	
D6	
D7	
Ø2	Phase two clock
R/W	
+8V	
−8V	
1200b	
600b	
300b	
150b	
110b	
RESET	
I/O SELECT	

Table 3. The S30 bus structure.

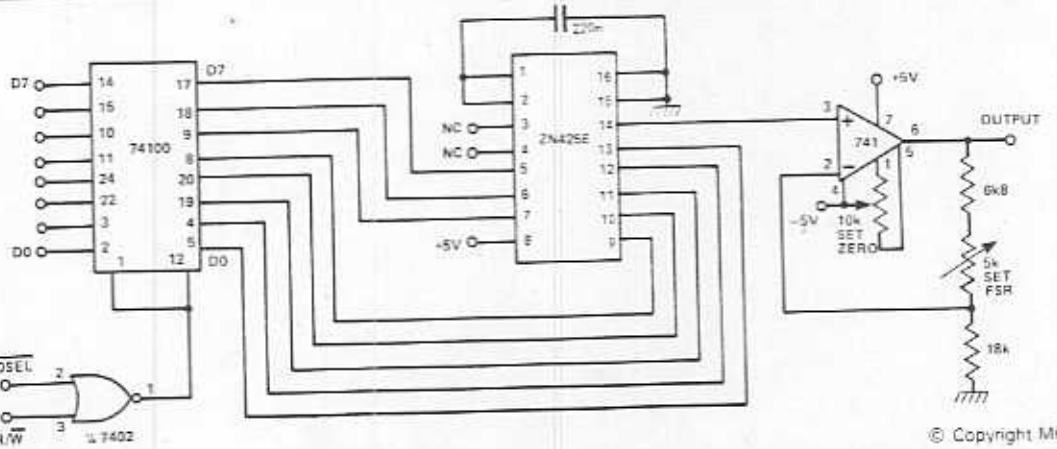
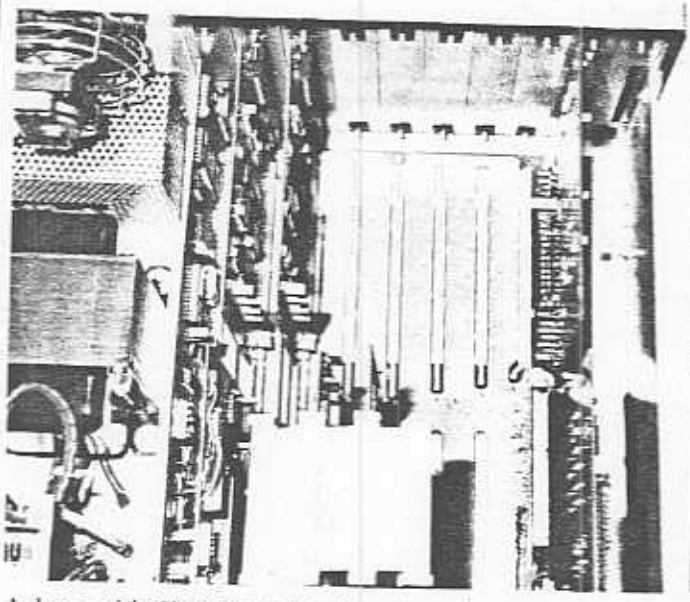


Fig.1 The simple analogue interface.



A close-up of the S30/S50 buses. Note the neat way the cards mount directly to the rear of the case allowing sockets to be easily fitted.

OLD S50 NAME	NEW S50C	COMMENTS
MRST	MRDY	Memory ready line (for slow memory)
NMI	BUSY	Bus in use
UD2	FIRQ	Fast interrupt request (New 6809 interrupt)
UD1	Q	Clock line
02	E	Clock line
01	BS	Bus status
110b	BUSRQ	Bus request
150b	S3	A19
300b	S2	A18
600b	S1	A17
1200b	S0	A16

Table 4. Changes on the S50C.

OLD S30 NAME	NEW S30C	COMMENTS
UD3	RS2	Register select line two
UD4	RS3	Register select line three
NMI	FIRQ	Fast interrupt request
600b	4800b	
150b	9600b	

Table 5. Changes on the S30C.

solves the problem of when to latch the data bus. The final circuit (including analogue components) can be seen in Fig. 1. It's as easy as that!

The Processors — 6800 And 6809

Another delight of the S50 bus is the 6800 microprocessor. The standard micro on the S50 may only have two accumulators (A and B registers), one index register (X), and a stack pointer, but its addressing modes are extensive and uniform. That is, every instruction (except for a few obvious exceptions) may use all of the addressing modes. All in all, the 6800 is a well designed processor that is easy to program in assembler code.

Recently Motorola has introduced the 6809 as a replacement for the 6800. With two accumulators, index registers and stack pointers, the 6809 is powerful. Its addressing modes include all of the 6800's plus many more. I would urge anyone considering a new processor to study the 6809 carefully rather than simply choosing a "standard" Z80. From the point of view of students and teachers the 6809 provides a good model of a well designed MPU — simple, elegant and complete. From the point of view of anyone considering real-time processing the 6809 is roughly one and a half times faster than a Z80 and a double speed version will be available soon. Clearly the 6809 will be with us for some time.

Extended Addressing

With the 6809 came the need to increase the addressing range of the S50 bus. Also some extra control lines used by the 6809 are not included in the S50 bus definition. These problems have been overcome by the S50C bus definition, the main features of which can be seen in Table 4, the corresponding new S30C bus definition is given in Table 5. The main improvements are the provision of four extra address lines, giving access to one megabyte of main memory, and two extra register select lines, giving each I/O port sixteen memory locations. These two details make the S50C bus ready for the next generation of micros. Comparing the S50C with the S50 definition indicates that S50/S30 devices will work on the S50C/S30C bus with little or no modification. Going the other way is not always so easy but some manufacturers make plug-in cards that can be used on both versions of the S50.

Software

Although most of this article has been about hardware characteristics of the S50/S50C bus, it would not be complete without a few words about software. In particular the most used operating system, FLEX, deserves a word of praise. So much has been written about CP/M and so little about FLEX that it would take a complete feature (or more) to describe the advantages that FLEX has over CP/M. From assembly language disc files can be created, renamed etc. with very little effort. FLEX is well documented and has a range of programming utilities (such as DEBUG, a 6800/6809 simulator). High level languages are also available and share most of FLEX's features. It is enough (for the moment) to say that all the software making up the FLEX system is user, rather than programmer, oriented.

The Future

At this point I hope I have convinced you that the S50 bus has advantages for some purposes. I would not suggest that the S50 was always the best — it too has its problems. In particular for the next generation of micros an eight bit bidirectional data bus will be too small. Whether another eight pins (or more) can be found is a matter of some doubt but, even so, a 68000 card for the S50 is scheduled for early this year. It is certainly true that the deficencies will become more apparent as time moves on but the S50 will always be a simple-to-use, and cheap, alternative to whatever else comes along.

With the introduction of the 6809, the S50 bus is becoming popular again and a great deal of new activity and interest is evident (viz 68' MICRO JOURNAL). Also, the advent of so many non-S100 bus machines, such as PET, Apple etc, means that the S50 stands a good chance of being used as much as, if not more than, the S100 in future.

The real strength of a bus standard that will endure for the future comes from the number of cards available and planned that can be used on it. To show that the S50 is healthy I include Table 6 — a list of S50 cards that I know about along with their availability. This list is by no means complete and I apologise to

any manufacturers whose products I may have omitted.

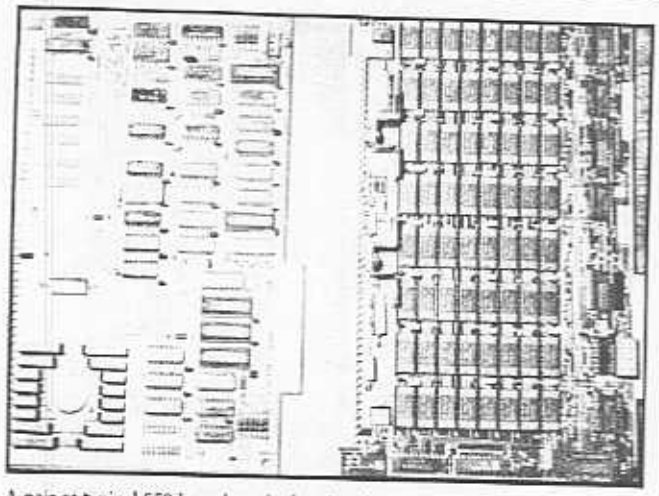
Conclusion

By this time it should be clear that I think the S50 bus plus the 6809 plus FLEX makes a good system. In particular:

*S50 cards are simple and cheap
*The S30 bus is easy to interface to a variety of devices
*A wide range of cards is in production
*A wide range of cards is planned for the future by a number of manufacturers
*The 6089 is an elegant and powerful processor
*FLEX is an elegant and powerful operating system
*Some excellent systems software is available (BASIC, Pascal, FORTRAN etc)

CARD	COMMENTS	AVAILABILITY
6800 CPU	At least three types	NOW
6809 CPU	Two current more planned	NOW
68000 CPU	Not much information yet	1st Q 1981
Memory	All types from 4K to 32K with many different features	NOW
SERIAL	One, two or eight channel RS232	NOW
PARALLEL	One or eight i20 bit channels	NOW
TIMERS	Interrupt and interval	NOW
EPROM PRG	Both 2716 & 2708	NOW
EPROM CARDS	Both 2716 & 2708	NOW
A to D's	Fast 12 and 8 bit types	NOW
D to A's	Fast 12 and 8 bit types	NOW
VDU CARD	With low res graphics	NOW
HIGH RES	High resolution graphics card	3rd Q 1980
DISC CONTROL	With drives for both 8" and 5"	NOW
DISC CONTROL	Without drives for 8" and 5"	3rd Q 1980
PROTOTYPE	S30 and S50	NOW
EXTENDER	S30 and S50	NOW

Table 6. What's available for the S50.



A pair of typical S50 based cards showing their compactness.

Our thanks are due to Computer Workshop of 38 Dover Street, London for providing photographic facilities.