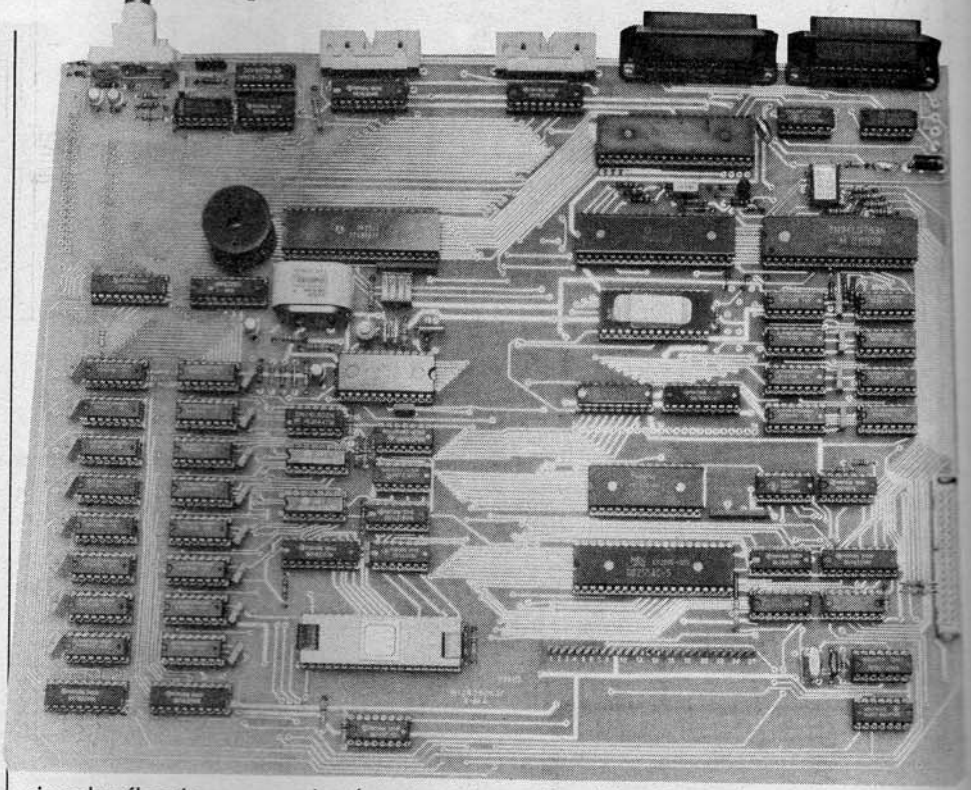
6809-BASED MICROCOMPUTER

Designer Dave Rumball takes us chip-by-chip through the circuitry of his single board computer.



This is the second in a series of articles which describe the design, construction and use of a powerful, 8-bit, single-board microcomputer based upon the 6809 microprocessor. The board uses the Flex operating system, giving access to a wide range of cross-assemblers and making it particularly suited to software development work. As well as having all the features usually found on a Flex standard machine, this design also offers very high resolution monochrome graphics, 128K of graphics RAM, a RAMdisc system which uses a variable amount of the 128K graphic RAM and appears to an operating system exactly as though it were a floppy disc, and an EPROMdisc system which consists of a small, plug-in board and again appears to the operating system as a floppy disc. Other features include a battery backed-up real time clock and an on-board EPROM programmer, and the complete package is available in kit form from Micro Concepts.

In this article we will look at the workings of the microcomputer section by section. In subsequent articles we will be describing the construction of the board and how to use it.

The CPU, Memory, Buffers And Decoding

The 'core' of the Microbox II is formed by the processor IC1, the SAM chip IC2 and the memory IC3-IC12. IC2 has several functions. First, it takes the master 16MHz clock from IC15 and generates the 1-2MHz processor clocks. The processor address is converted to the multiplexed eight-bit buss and control strobes necessary for the eight 64K DRAMs, IC5-IC12. 22 ohm resistors in these lines damp any signal reflections or undershoots which would disturb the DRAM operation. It also defines a three-bit decoding buss which is used by the decoding logic. An 8K EPROM, IC3 holds the monitor program and system service. IC4 buffers the DRAM read data onto the processor data buss, whilst IC13 is a bi-directional buffer between the processor and the peripheral data busses.

The low order address lines, the control strobes E and R/W, and the reset signal are buffered by IC18, which has its two enable signals grounded. The reset signal from SW2 triggers two time constants, the shorter of which resets the SAM chip by pulling VCLK low, whilst the longer resets the processor so that the SAM chip comes out of reset before the processor. Note that no use is made of the SAM chip's video capabilities in this design.

The HS pin is tied low on the SAM chip. This frees up an extra RAM cycle per CPU cycle allowing operation at 2MHz. However the SAM chip stops refreshing the DRAM at 2MHz, so operation at this speed can only be for periods of less than 2ms, or longer if the operation itself refreshes the memory as would a transfer of 256 bytes during a disc operation.

The memory system map is defined by IC65 and parts of IC14 and IC16. The memory map is filled with the 64K RAM, except for the top 8K section which is the monitor EPROM. This 8K section is split into two, and the bottom 4K may be switched between EPROM and RAM with the MAP signal from the system PIA. This is used in the current software to

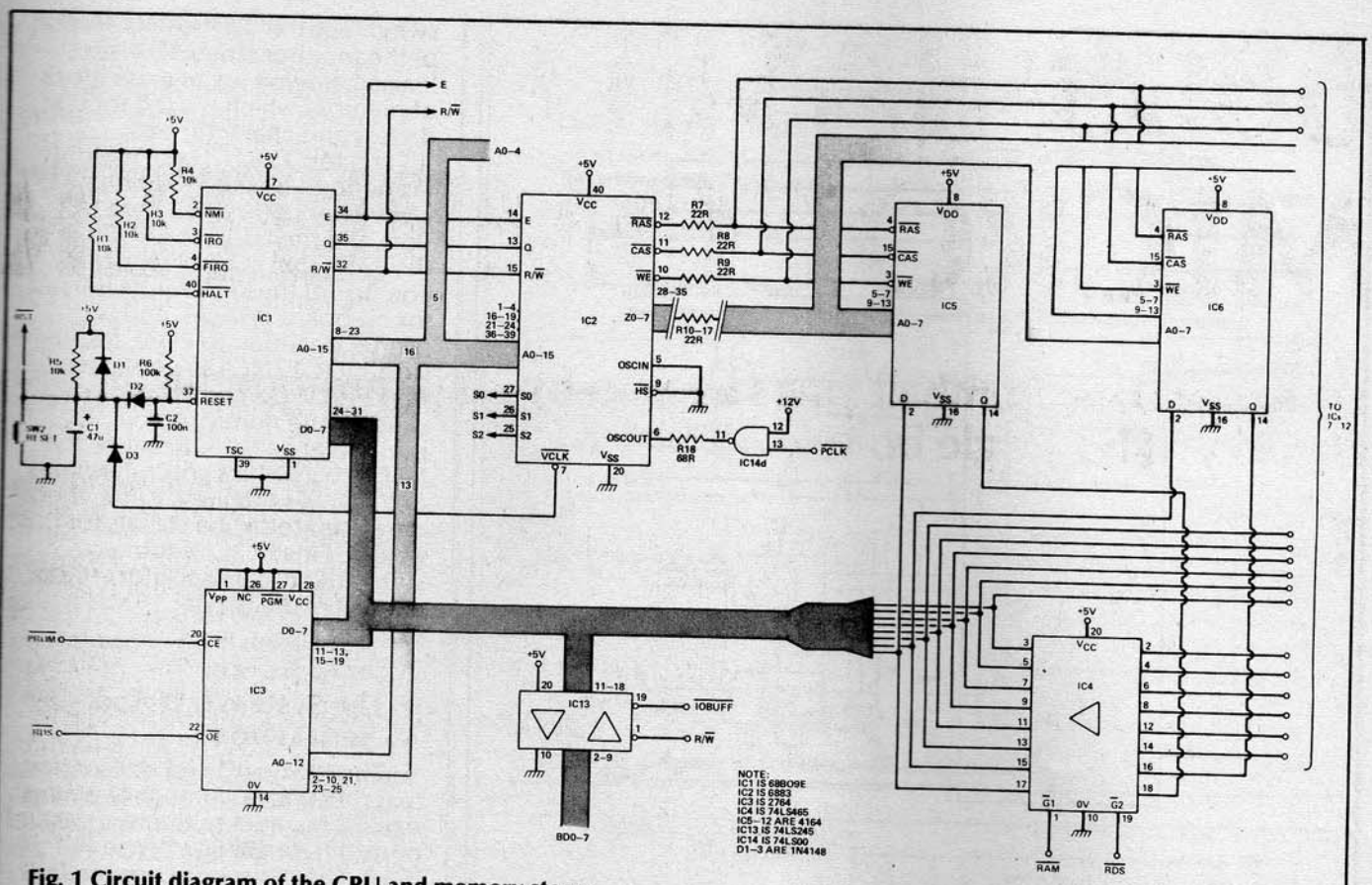


Fig. 1 Circuit diagram of the CPU and memory stages.

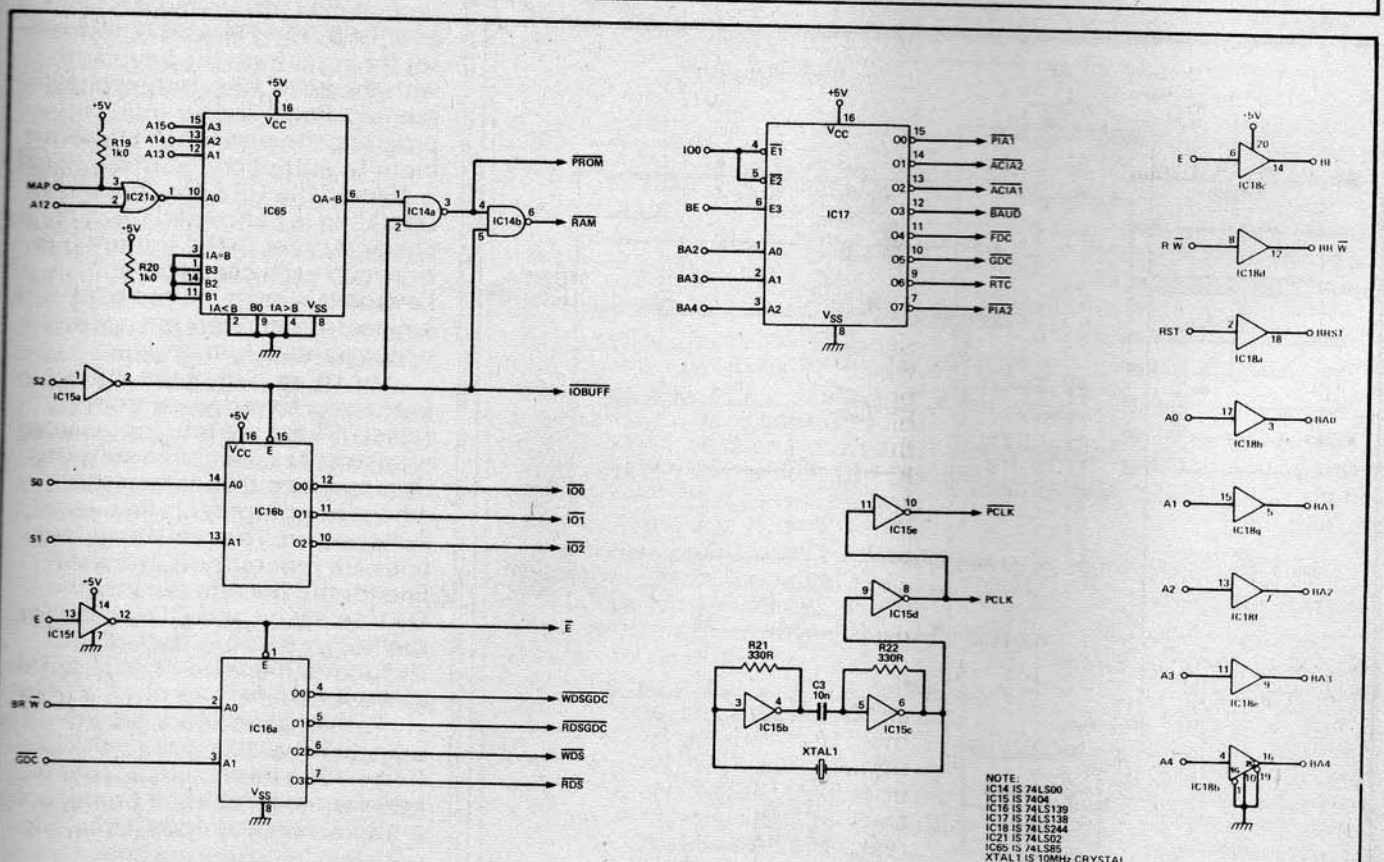


Fig. 2 Circuit diagram of the decoding, buffers and master clock.

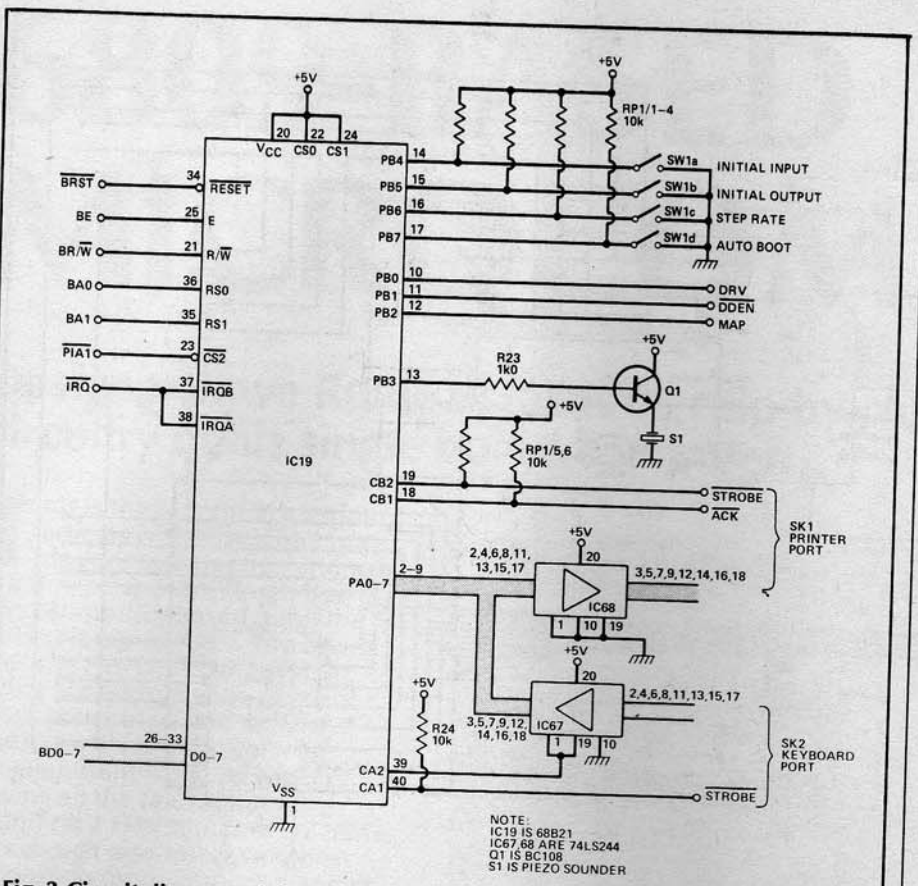


Fig. 3 Circuit diagram of the system interface.

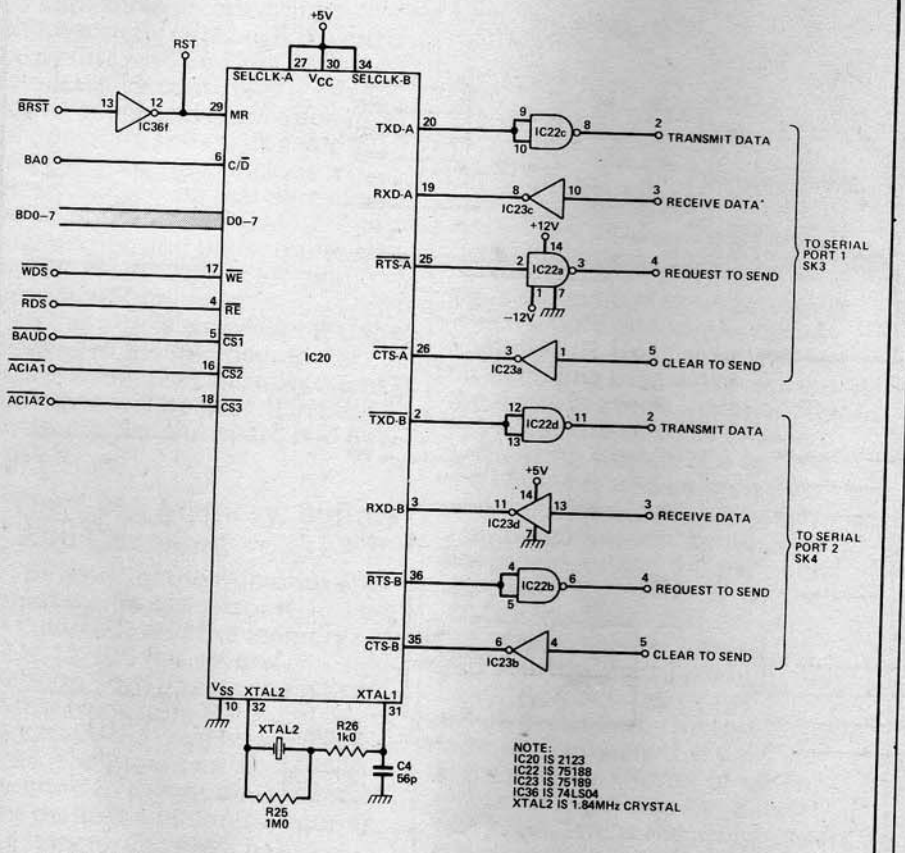


Fig. 4 Circuit diagram of the serial ports.

switch out the diagnostics section of the monitor when Flex is loaded, freeing up an extra block of memory which is used for text drivers and character sets.

The top 256 bytes of memory (as defined by the SAM chip) are given over to three 32 byte I/O slots and the addresses used to set the SAM chip control registers. The first of these I/O slots is used for on-board devices, and is further decoded to eight, four-byte slots by IC17. IC16a generates the RDS and WDS control strobes used by the non-Motorola peripheral devices. Because the NEC720 graphics controller does not have a separate CE line, there are separate strobe signals for this device. Finally, IC15 forms a standard crystal oscillator which generates the master 16MHz clock.

The System I/O And Serial Ports

The keyboard and printer ports, together with a number of control signals, connect to the two parallel ports of a single 6821 type PIA, IC19. The centronics printer and parallel keyboard share the first port via two tristate buffers IC67 and IC68. The PIA port is normally set for input from the keyboard, with the keyboard strobe going to the CA1 line. When printing is in progress, the port is turned from input to output and a strobe signal is sent on the CB2 line. This operation is performed for each character sent to the printer — in between each character, the keyboard is examined so that keyboard characters are not lost whilst printing is in progress.

The other port of the PIA is given over to various system signals. There are four inputs from four switches which the software uses to set certain parameters when the computer is first switched on. The remaining four lines are four outputs, the MAP line for the decode section, the DRV select bit and DDEN line for the floppy disc interface, and a signal which enables a sounder to give a 'beep'.

The serial ports are provided by a single IC, a WD2123 DUART (IC20). The internal baud rate generators derive their timing from a 1.84 MHz crystal oscillator. The data and handshaking lines are buffered from TTL to RS-232 levels and back again by the obligatory 75188/75189 pair.

The Floppy Disc Interface and PROMdisc

The floppy disc controller is refreshingly simple: it consists of just three ICs, two of which are SSI buffers! The work is done by IC24, a WD1770 floppy disc controller, which connects directly to the peripheral data buss. Input signals from the drives are buffered by IC25, whilst output signals are buffered by IC26. The two drive select lines are derived from a single signal. This means that one drive or the other will be selected all of the time, and its drive select light will be on. This causes no harm if the drive is set up to load its head with the MOTOR ON signal. The drive motor timing is set by the 1770 by counting index pulses. It will stop the drive nine index pulses after the last operation, and will delay any operation until six index pulses have occurred.

The EPROM disc is formed from an 8255 PIA, four EPROMs and an eight bit counter. The data lines from the EPROMs are connected to one of the ports of the PIA, IC28, and the high eight address lines for the EPROMs to another. Chip enables for the four EPROMs, the program line for one of them, and clear and count lines for the counter are connected to the last port. Because Flex only reads data from discs in chunks of 256 bytes, not every address line is needed and the low eight address lines can come from an eight bit counter. To read a 'sector', the processor selects the correct EPROM as a function of the 'track' and 'sector' numbers, then clears the counter and clocks it 256 times, moving each byte for the port to RAM as it goes.

EPROMS may be programmed by applying 21V to the VPP pin, setting the address lines and data, and then pulsing the program line for 50ms.

The operation of the remainder of the board will be described next month, when we also hope to bring you complete constructional details including board overlay and parts list. If you'd rather not wait that long, a kit of parts complete with full constructional details is available from Micro Concepts, 2 St. Stephens Road, Cheltenham, Gloucestershire GL51 5AA, tel 0242- 510 525.

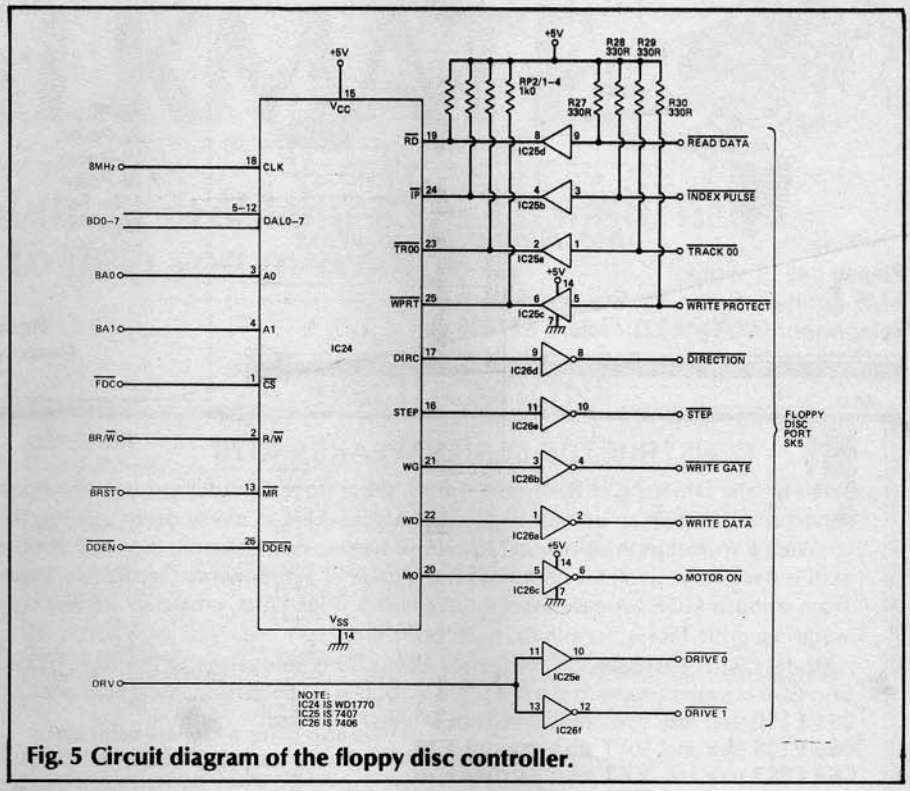


Fig. 5 Circuit diagram of the floppy disc controller.

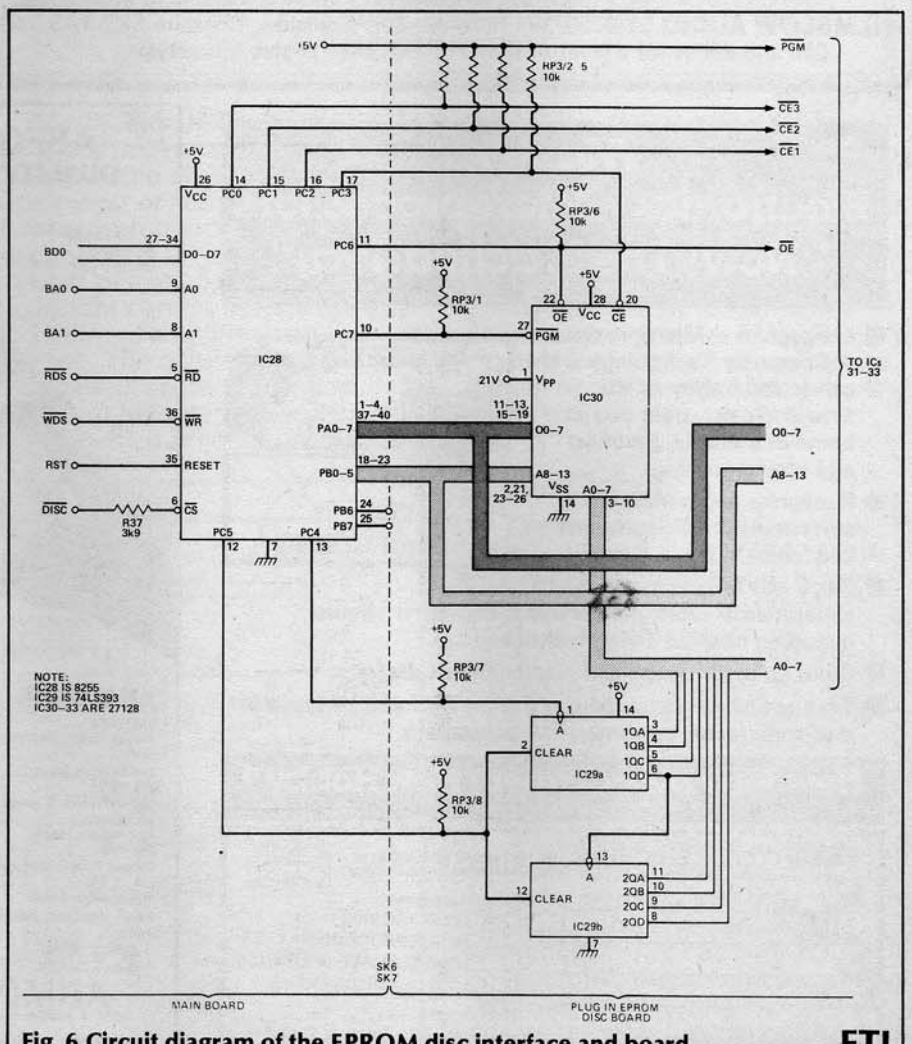


Fig. 6 Circuit diagram of the EPROM disc interface and board.

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