

Fig. 1 Circuit diagram of the CPU and memory stages.

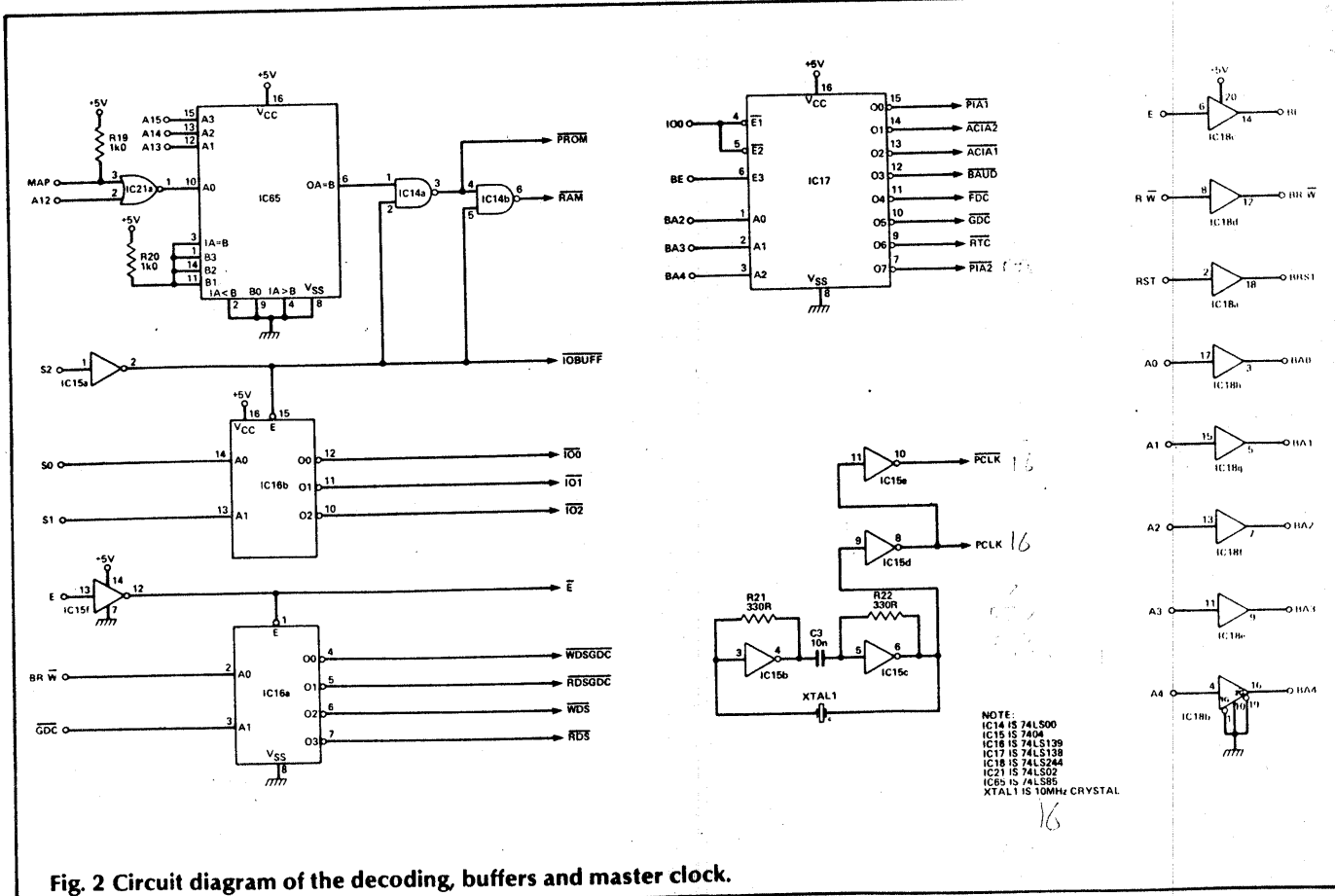


Fig. 2 Circuit diagram of the decoding, buffers and master clock.

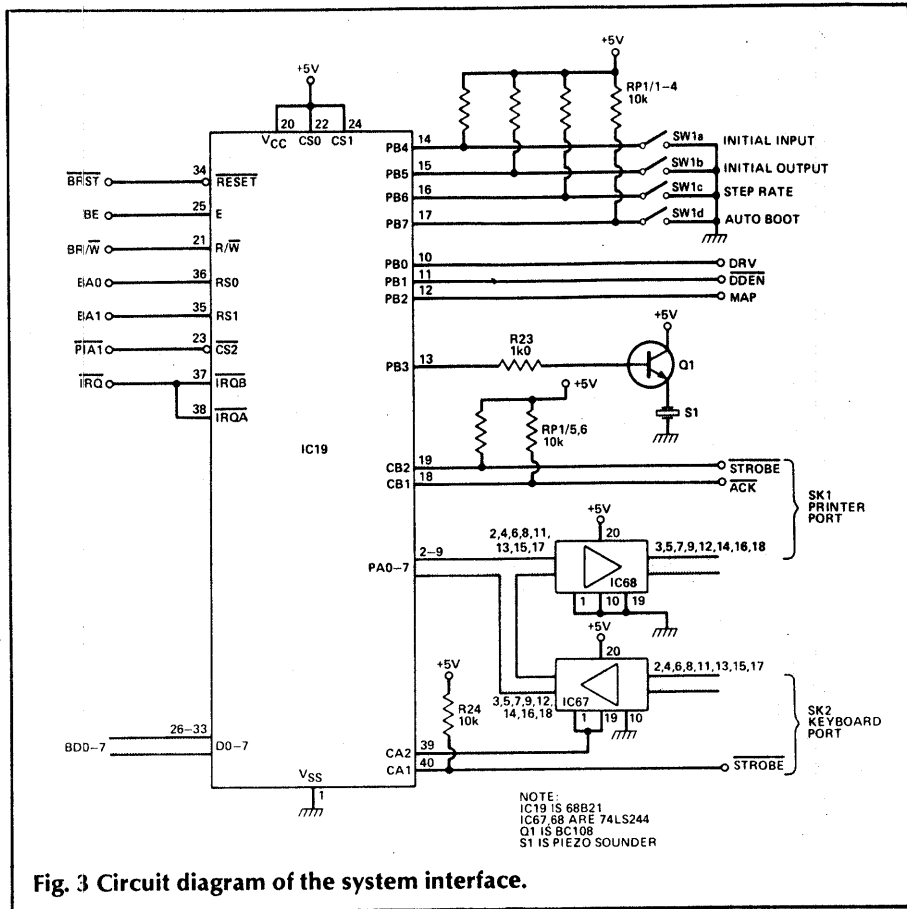


Fig. 3 Circuit diagram of the system interface.

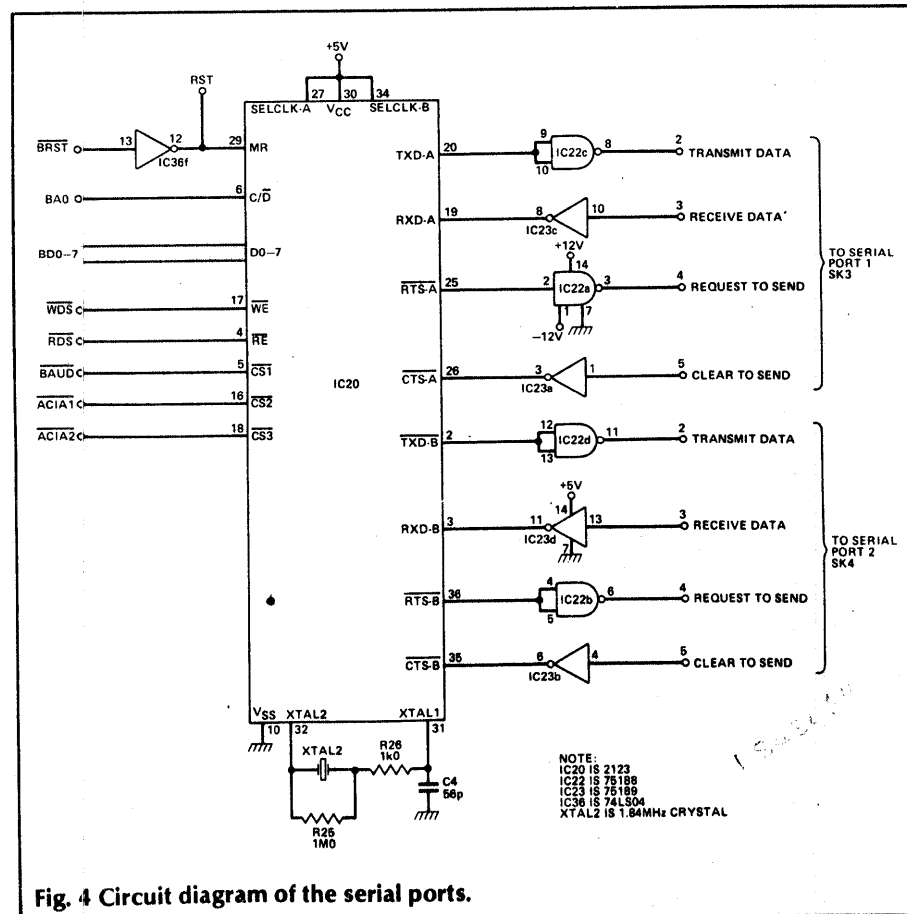


Fig. 4 Circuit diagram of the serial ports.

switch out the diagnostics section of the monitor when Flex is loaded, freeing up an extra block of memory which is used for text drivers and character sets.

The top 256 bytes of memory (as defined by the SAM chip) are given over to three 32 byte I/O slots and the addresses used to set the SAM chip control registers. The first of these I/O slots is used for on-board devices, and is further decoded to eight, four-byte slots by IC17. IC16a generates the RDS and WDS control strobes used by the non-Motorola peripheral devices. Because the NEC720 graphics controller does not have a separate CE line, there are separate strobe signals for this device. Finally, IC15 forms a standard crystal oscillator which generates the master 16MHz clock.

The System I/O And Serial Ports

The keyboard and printer ports, together with a number of control signals, connect to the two parallel ports of a single 6821 type PIA, IC19. The centronics printer and parallel keyboard share the first port via two tristate buffers IC67 and IC68. The PIA port is normally set for input from the keyboard, with the keyboard strobe going to the CA1 line. When printing is in progress, the port is turned from input to output and a strobe signal is sent on the CB2 line. This operation is performed for each character sent to the printer — in between each character, the keyboard is examined so that keyboard characters are not lost whilst printing is in progress.

The other port of the PIA is given over to various system signals. There are four inputs from four switches which the software uses to set certain parameters when the computer is first switched on. The remaining four lines are four outputs, the MAP line for the decode section, the DRV select bit and DDEN line for the floppy disc interface, and a signal which enables a sounder to give a 'beep'.

The serial ports are provided by a single IC, a WD2123 DUART (IC20). The internal baud rate generators derive their timing from a 1.84 MHz crystal oscillator. The data and handshaking lines are buffered from TTL to RS-232 levels and back again by the obligatory 75188/75189 pair.

6809-BASED MICROCOMPUTER

Dave Rumball and Gary Mills conclude their description of the workings of the computer before going on to consider the choices facing constructors and the assembly of the two boards.

The real time clock, IC27, is a 146818. This part is designed for a multiplexed processor address/data bus, but here is used with a non-multiplexed processor by means of a separate address decode for the address and data strobes. The CE line is grounded by a transistor which is held on by the main +5V rail. When the system power fails, the chip is disabled in order to prevent corruption of the data. The clock has its own internal oscillator which is driven by a 32.768 kHz crystal to reduce power consumption. Power for the clock is provided by a trickle-charged NiCad battery when the main power is off.

The 146818 also contains 64 bytes of CMOS RAM which are used to hold various system parameters, such as the serial baud rates, video timing parameters etc. An RC network on the PS input gives an indication of battery failure. The software checks for this condition on power up and loads a default set of system parameters if the battery power has failed.

The Display Section

The display section consists of three parts, the NEC7220A graphics controller IC34, a 128K bank of DRAM, ICs47-62 (not part of the processor address space), and some control logic. The NEC7220A does 98% of the work in producing the video. It generates the correct display address for the RAM, master timing strobes for reading and writing to the RAM, and display blanking and synchrony signals. The sixteen bit display address is multiplexed onto the eight bit RAM address by

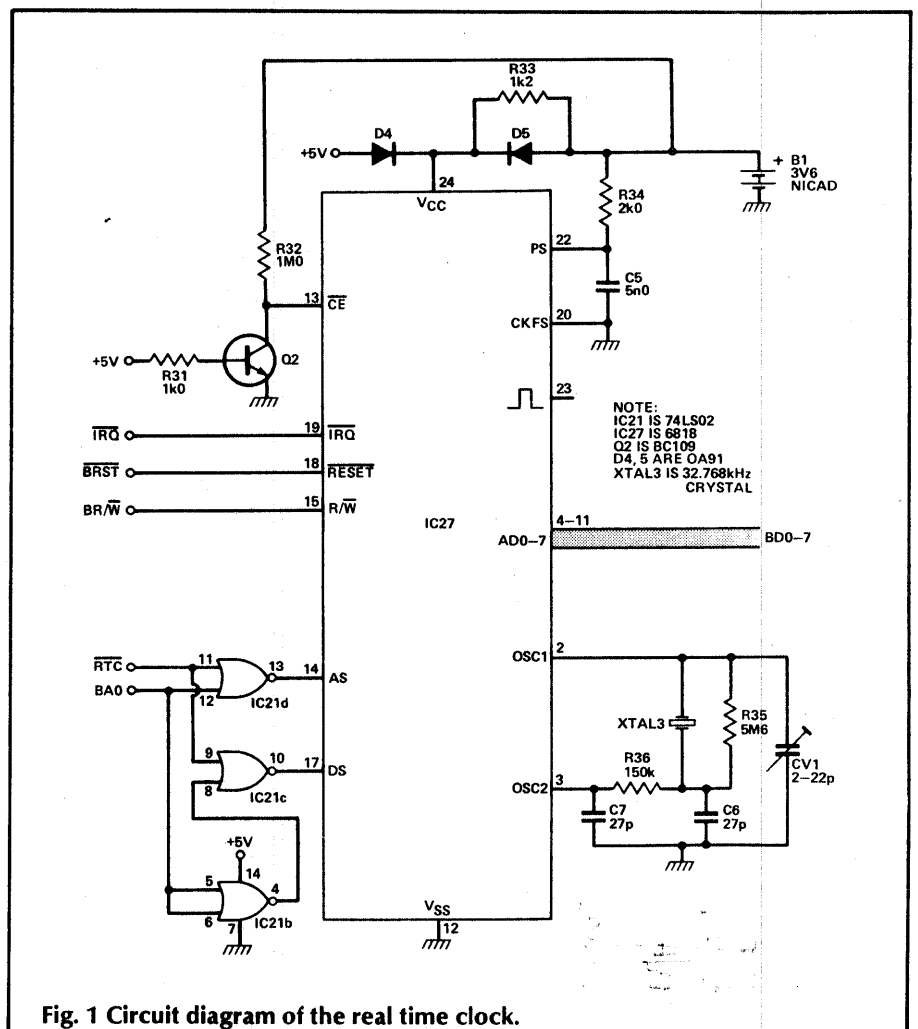


Fig. 1 Circuit diagram of the real time clock.

OOPS!

A capacitor should be added to the serial interface controller oscillator circuit shown in Fig. 4 on page 38 of last month's issue. The capacitor is C30, a 27p polystyrene type, and should be connected between pin 32 of IC20 and the 0V line. It

has been included in the overlay diagram and the parts list in this article.

In Fig. 2 on page 37 of the January issue, XTAL1 is listed as a 10MHz crystal. It should be a 16.000MHz crystal, as stated in the parts list in this article.

Fig. 2 circuit diagram of the graphics and RAMdisc section.

NOTE: 7720A
 IC38 IS 74LS175
 IC39 IS 74LS175
 IC37 IS 74LS194
 IC38 IS 74LS194
 IC39 IS 74LS194
 IC40 IS 74LS163
 IC41 IS 74LS21
 IC43, 44 ARE 74LS257
 IC45, 46 ARE 74LS244
 IC47 IS 74LS244
 IC53, 54 ARE 74LS200
 IC56 IS 74LS273
 CS, 4 ARE 2N2236A
 DS, 7 ARE 1M148
 ZD1 IS 0V8

