

$P_o$  is the output power from the transistor.  $V_o$  is the peak fundamental component of the collector voltage swing ( $V_{ce} - V_{ce0}$ ) and is typically 11V for a 12V supply or 26V for a 28V supply. For Class A operation

$$R_L = \frac{V_o I_c}{I_c}$$

where  $V_{ce}$  and  $I_c$  are the dc values of collector voltage and current.

**Design of matching networks**

The low impedances encountered in semiconductor amplifiers require a different design approach compared with valve counterparts. pi networks, parallel-tuned circuits and high-Q lines, popular with valve designs, give rise to impractical component values when scaled for transistor impedances. Suitable networks for use with transistors are given in Fig 25 together with appropriate formulae. These networks give rise to practical components at vhf and uhf up to about 800MHz.

Above 400MHz an alternative approach to matching is to use sections of microstrip transmission lines fabricated on printed circuit board. These networks are most conveniently designed using transmission-line impedance plots such as the Smith chart. Networks of this form may be used well into the microwave region. To provide for variations in tuning and matching of the networks shown in Fig 25, two components should be made variable. This is most easily accomplished with trimmer capacitors.

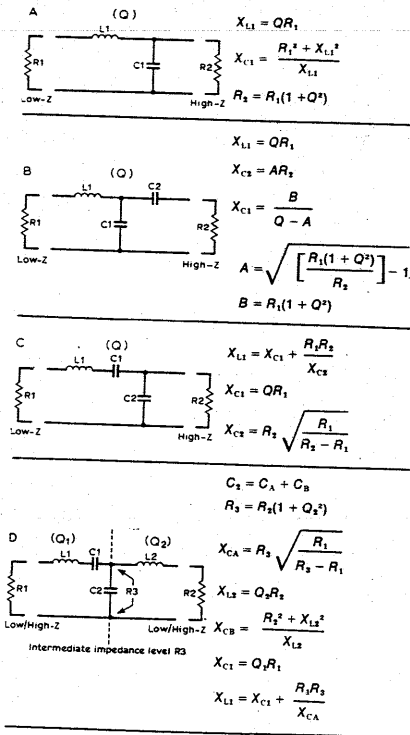
Double pi and L-pi networks can also yield practical values if the intermediate impedance level is suitably selected (around 1,000Ω). These networks can give rise to excellent harmonic rejection. Output networks which have an inductive element connected to the transistor such as those in Fig 25, give rise to higher efficiencies than those which have a capacitive shunt feed. This is due to the nature of the impedance presented to the device at harmonic frequencies.

The loaded Q of the network should be typically in the range 3 to 12. High-Q networks give better harmonic rejection but result in higher circulating currents, higher voltages, greater losses and are more critical on tuning. For high-power stages or where large impedance transformation is involved, it is often preferable to use two cascaded low-Q networks rather than one high-Q network. A suitable combination from Fig 25 is A nearest the transistor followed by B or C. The intermediate impedance level should lie between the source and load impedances and can be conveniently the geometric mean

$$R = \sqrt{R_1 R_2}$$

Impedance is usually quoted in published data as either a series combination of resistance and reactance  $Z = R + jX$  or a parallel combination of conductance and susceptance  $Y = G + jB$ . It is often necessary to convert from series to parallel and vice versa. The following relationships may be used (Fig 26).

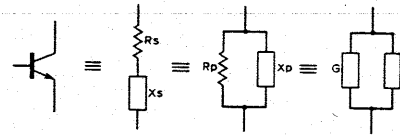
$$\begin{aligned} Z &= R + jX & Y &= G + jB \\ Y &= \frac{1}{Z} & R_p &= \frac{1}{G} & X_p &= -\frac{1}{B} \\ R_s &= \frac{R_p X_p^2}{R_p^2 + X_p^2} & X_s &= \frac{R_p^2 X_p}{R_p^2 + X_p^2} \\ R_p &= \frac{R_s^2 + X_s^2}{R_s} & X_p &= \frac{R_s^2 + X_s^2}{X_s} \end{aligned}$$



**Fig 25. Tuning networks for transistor rf power amplifiers.** (a) Simple L-network which often lacks flexibility, and will only match unequal impedances. (b) and (c) are ideal for transistor input/output tuning networks but will only match between unequal impedances. In (d)  $Q_1$  and  $Q_2$  need not be the same. The intermediate impedance level is higher than  $R_1$  or  $R_2$ . This network is ideal for matching near-equal impedances

For a capacitor  $jX$  will be negative and  $jB$  will be positive. For an inductor  $jX$  will be positive and  $jB$  will be negative. If  $X_s$  is a capacitive reactance,  $X_p$  will also be a capacitive reactance and similarly for inductive reactances.

Fig 27 shows a typical design for a vhf power amplifier. The input network is required to match from typically 50Ω, or from the load impedance of the previous stage, to the input impedance of the device  $R_i + jX_i$ . The value of  $R_i$  is used in the design formulae B. The value calculated for  $L_1$  should be reduced by an amount  $X_i$  if the input impedance is inductive ( $jX_i$ , positive) or increased by an amount  $X_i$  if the input impedance is capacitive ( $jX_i$ , negative). It is often the case with



**Fig 26. Series-to-parallel conversions**

high-power devices and low input impedances that a single network solution will not be possible at moderate Q values. By placing capacitors directly from base to emitter an L network is formed with the transistor bond wires, raising the input impedance to a manageable level. At uhf, where  $X_i$  can be large compared with  $R_i$ ,  $X_{L1} - X_i$  can result in impractically small values for  $L_1$  and again the solution is to place capacitors directly from base to emitter to form an L-network with the transistor bond wires. Some fixed capacitance from base to emitter is often desirable on grounds of stability in any case.

The output network is required to match from the calculated value of  $R_L$  to the load impedance which is typically 50Ω.  $L_3$  should resonate with the parallel output capacitance of the transistor obtained from the data.

$$2\pi f L_3 = \frac{1}{2\pi f C_{out}}$$

The value of  $L_3$  is non-critical as the loaded Q of this parallel circuit is very low. Keeping the value of  $L_3$  to a minimum will enhance the overall stability. Component values for  $L_4$ ,  $C_3$  and  $C_4$  can be obtained from Fig 25.

**Example**

Mullard BLY89A operating as a 25W fm amplifier at 144MHz used in the circuit described and operating between 50Ω source and loads. Supply voltage 12.5V.

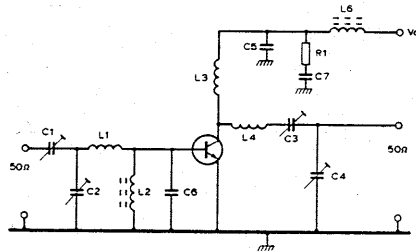
From published data  $Z_i = 1.7 + j1.4\Omega$ ;  $C_L = 65pF$ ;  $V_{ce} = 12.5V$ ;  $V_o$  typically 11V;

$$R_L = \frac{V_o^2}{2P_o} \quad R_L = 2.4\Omega$$

Select  $Q = 10$  for both input and output networks. Output network must match 2.4Ω to 50Ω.

From Fig 25(c),

$$\begin{aligned} X_{C3} &= 24\Omega; X_{L4} = 34.7\Omega; X_{C4} = 11.2\Omega \\ L_3 &\text{ must resonate with } C_L = 65pF \text{ at } 144MHz. \\ X_{L3} &= 17\Omega. \end{aligned}$$



**Fig 27. Typical circuit of vhf power amplifier**

The input network must match 50Ω to  $1.7 + j1.4\Omega$ . This corresponds to a resistor of 1.7Ω in series with an inductive reactance of 1.4Ω.

From Fig 25(b), to match 1.7Ω to 50Ω,

$$X_{C1} = 78\Omega; X_{L2} = 20.3\Omega; X_{L1} = 17\Omega$$

To account for the 1.4Ω series inductance seen at the transistor base terminal, this value must be subtracted from  $X_{L1} = 17\Omega$  to give  $X_{L1} = 15.6\Omega$ .

Inductance and capacitance values can be found from

$$L = \frac{X}{\omega} \quad \text{and} \quad C = \frac{1}{\omega X} \quad (\omega = 2\pi f)$$

**Components list:** C1 14pF; C2 54pF; C3 46pF; C4 98pF; L1 17nH; L3 19nH; L4 38nH.

**Practical amplifier construction**

The simplest and most reliable method of constructing a vhf power amplifier is to use a printed circuit board. In double-sided glassfibre board is suitable for use up to 432MHz. PTFE loaded board is desirable at higher frequencies. Fig 28 shows a typical layout adopted for the amplifier shown in Fig 27. It is most important to keep stray inductances to a minimum, particularly the emitter lead inductance.

The underside of the board should be plain copper used as the earth plane and grounding points taken through the board using copper tabs or rivets at every point where a component connects to ground. The most satisfactory method of grounding the emitters is to wrap copper foil through the transistor locating hole to connect the emitter leads directly to the earth plane at a point where the leads emerge from the body of the transistor (Fig 29). The printed board should be supported to avoid strain or flexing of the transistor leads (Fig 30).

Components for the matching networks should be selected for high current capability, low loss and low lead inductance. For fixed capacitors, npo ceramic tubular or plate capacitors are suitable but miniature types should be avoided. At high power levels it will be necessary to use porcelain chip or mica capacitors. Decoupling capacitors should be low-inductance types such as feedthrough capacitors. For trimmer capacitors, professional-grade film dielectric trimmers are suitable for use up to 432MHz, and for higher capacitance values mica compression trimmers are suitable at lower vhf. Inductors can conveniently be wound self-supporting using bare copper wire. The wire diameter should be as large as possible. On 432MHz, the small inductance values often required may be easier to fabricate using copper strips on the circuit board. These may be designed with the aid of the charts in the Appendix. Base chokes should be of low Q to improve stability. For 144MHz, a suitable choke can comprise 1.5 turns of enamelled copper wire wound through a ferrite bead such as FX1115.

Several precautions may be taken to ensure stability. The layout should ensure that input and output networks are adequately isolated and low grounding impedances are achieved. A low-Q base choke should be used, possibly with extra damping in the form of a resistor of 5 to 22Ω connected base to ground. Referring to Fig 27,  $C_5$  should have a low impedance at the operating frequency but not at low frequencies.  $R_1$  and  $C_7$  ensure low-frequency stability.  $R_1$  should be a few ohms and  $C_7$  should have a reactance of a few ohms at a frequency of several hundred kilohertz. Typically  $R_1$  can be 4-7Ω and  $C_7$  100nF.  $L_6$  may be a ferrite choke with adequate dc current handling for the power levels involved. For high-gain devices operated well below  $F_c$ , it may be necessary to add some capacitance from collector to ground. Some fixed capacitance

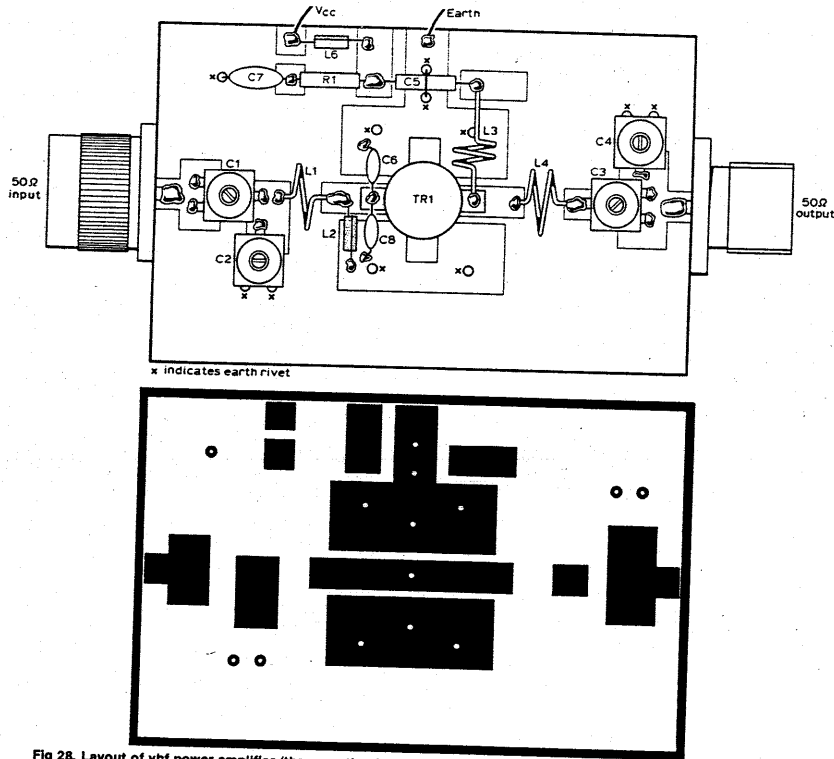


Fig 28. Layout of vhf power amplifier (the mounting hole for TR1 breaks the central conductor into two sections)

added base to emitter will often improve stability. Two capacitors should be used, one to each emitter lead, keeping lead lengths to an absolute minimum.

Multi-stage amplifiers should not present any particular problems. Interstage matching should be designed to match from the collector impedance of one stage to the base impedance of the following stage. It is often convenient to use two matching networks with a 50Ω intermediate impedance level.

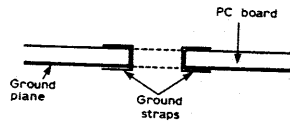


Fig 29. Earthing straps for the emitters

This enables the individual stages to be tested separately. Multi-stage amplifiers should be constructed in a single line to eliminate mutual coupling problems.

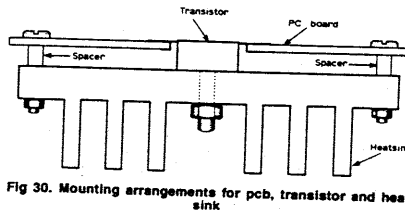


Fig 30. Mounting arrangements for pcb, transistor and heat sink

Alignment of the amplifier should be done initially at reduced drive and supply voltage while monitoring the supply current. The input network trimmers C1 and C2 should be adjusted for best input match (zero reflected power on a reflectometer) and the output network trimmers C3 and C4 should be adjusted for maximum output power. Once the networks have been initially aligned and the amplifier appears to be stable, the drive and supply voltage may be increased and the alignment procedure repeated in steps to the required operating levels. Stability may be checked by listening on a loosely coupled receiver for any unwanted spurious signals, noise or modulations. In addition, alteration of the trimmers or varying the drive or supply voltage should result in smooth variations of supply current and output power with no steps or jumps. Cascaded Class C stages will tend to have a switch on/switch off characteristic as the drive is reduced to zero. This should not be confused with instability.

**Higher powers**

Higher power levels may be achieved in a number of ways. The most obvious method is to use the largest available device. The limit from a single device is about 100W at vhf.

Transistors may be operated in parallel provided certain precautions are taken to achieve correct power sharing. The devices should be matched and a symmetrical layout adopted. The devices should be close together and tightly coupled thermally on the same heat sink.

Paralleling should not be attempted directly at the base or collector but should occur at a higher-impedance point. This implies using separate L-networks on the base and collectors for the individual transistors and then paralleling through a common matching network which may contain adjustable elements. Common-mode resistors may be added base-to-base and collector-to-collector (10–47Ω is typical). The number of devices paralleled should be limited to two.

Push-pull operation may be used, although network design becomes complicated. Impedances are four times higher than the equivalent parallel case. Push-pull operation is convenient to use with wideband ferrite-cored transformers. This mode of operation is popular at hf but may also be used at low vhf, particularly 70MHz.

Hybrid couplers may be used to couple two or more complete amplifier stages in parallel. It is important that the amplifiers are identical in terms of power output and phase characteristics. Hybrid couplers have the advantage that each amplifier is isolated from its counterparts and failure of one amplifier will still result in continued operation although at a lower power level. Solid-state vhf broadcast transmitters are constructed along these lines. There are various types of hybrid coupler that are suitable—hybrid ring coupler, Wilkinson multi-port combiner and the 3dB quadrature coupler. Hybrid ring and Wilkinson couplers may be constructed from  $\lambda/4$  and  $3\lambda/4$  lengths of coaxial cable.

**Bias units for linear operation**

For ssb operation, forward biasing of amplifier stages into Class AB is required. A suitable quiescent current is often 50–100mA. Low-distortion amplification requires that a low-impedance bias unit is used and two such circuits are shown in Figs 31 and 32. The diode biasing system is suitable for low power levels only. The bleed current through the series resistor must be greater than the peak bias current demand of the amplifier stage.

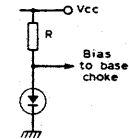


Fig 31. Diode biasing for Class AB amplifiers

$$R < \frac{(V_{cc} - 0.8) h_{FE}}{I_c}$$

where  $I_c$  is the dc collector current drawn by the amplifier under sustained p.e.p. conditions and  $h_{FE}$  is the current gain of the transistor at this current level. It is important that the diode is mounted in tight thermal contact with the amplifier transistor to prevent possible thermal runaway and maintain a constant quiescent collector current with variations in temperature.

The circuit shown in Fig 32 is capable of superior results and lower internal impedance. With the component values shown, it will provide 0.5A bias current. TR1 should be mounted in thermal contact with the amplifier transistor to prevent thermal runaway as before. TR2 will require heat sinking and can conveniently share the same heat sink as TR1 and the amplifier transistor.

**Heat sinks**

Adequate cooling should be provided to keep power devices well within their rated specification. Maximum junction temperature is normally quoted in published data as typically 200°C. This should not be exceeded under any condition. Knowing the total power dissipation and thermal resistances of the device and heat sink it is possible to calculate the maximum junction temperature.

Referring to Fig 33,  $\theta_{mh}$  is the thermal resistance of the crystal and header. This is quoted in published data and varies from typically 25°C/W for small metal-cased TO5 devices down to 0.8°C/W for large flange- or stud-mounted devices.  $\theta_{mh-h}$  is the thermal resistance of the interface between the mounting base of the device and the heat sink. This figure can be reduced considerably by the application of a thin smear of heat sink

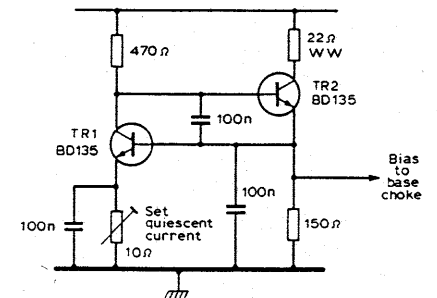


Fig 32. Low-impedance transistor bias unit for Class AB amplifiers

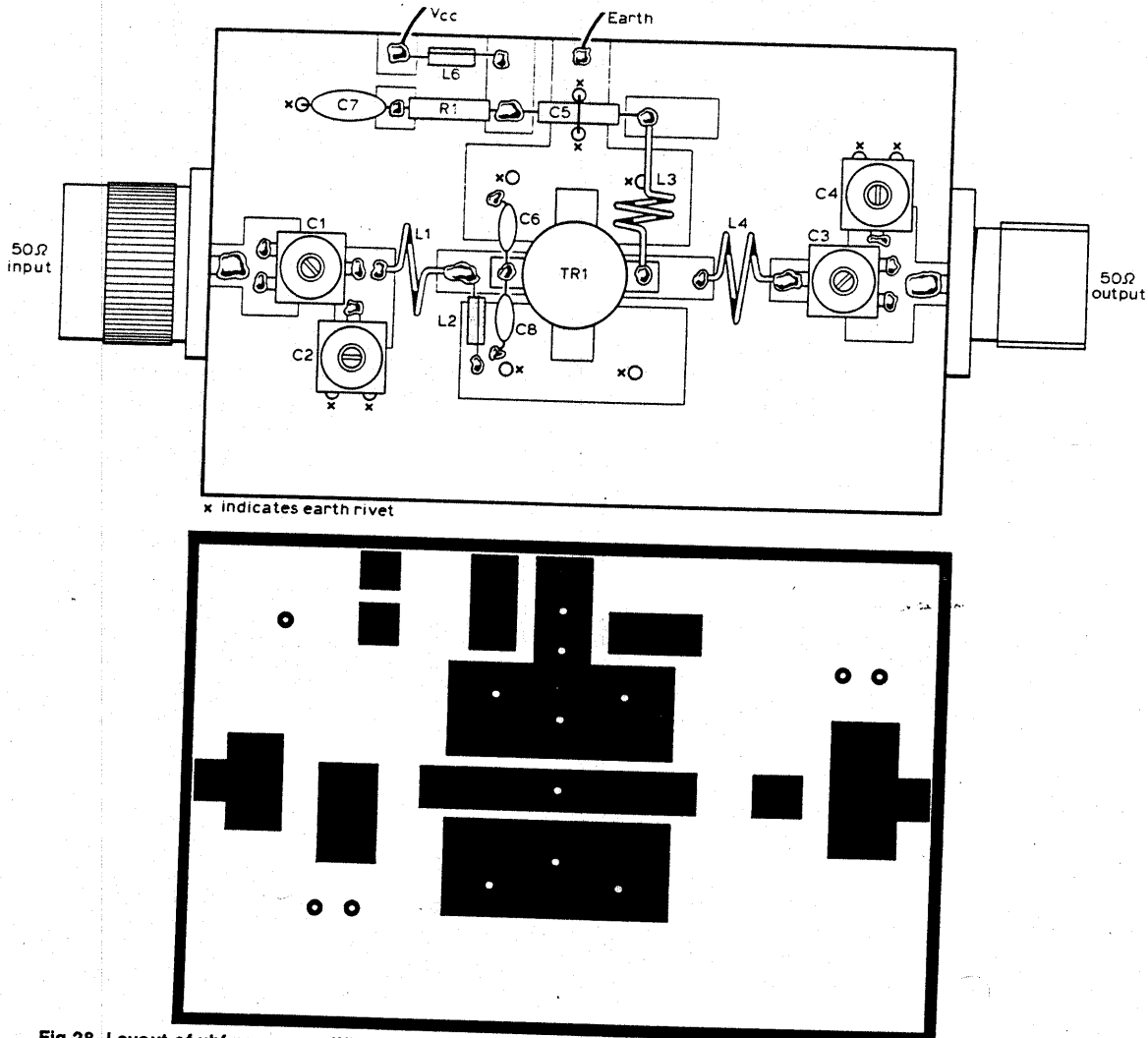


Fig 28. Layout of vhf power amplifier (the mounting hole for TR1 breaks the central conductor into two sections)

added base to emitter will often improve stability. Two capacitors should be used, one to each emitter lead, keeping lead lengths to an absolute minimum.

Multi-stage amplifiers should not present any particular problems. Interstage matching should be designed to match from the collector impedance of one stage to the base impedance of the following stage. It is often convenient to use two matching networks with a 50Ω intermediate impedance level.

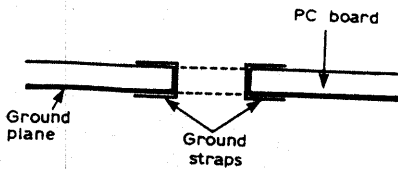


Fig 29. Earthing straps for the emitters

This enables the individual stages to be tested separately. Multi-stage amplifiers should be constructed in a single line to eliminate mutual coupling problems.

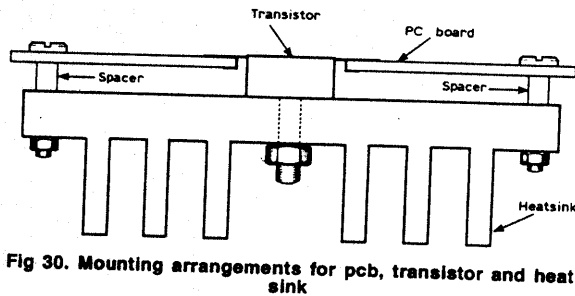


Fig 30. Mounting arrangements for pcb, transistor and heat sink

Alignment of reduced drive and current. The input should be adjusted for best in (with a meter) and the output should be adjusted for maximum power. If the drive is not initially stable, the drive should be adjusted for maximum power levels. Stability should be checked for modulations. In addition, the drive or supply current should be checked and the supply current and the Class C stage characteristic as the amplifier is confused with inst

**Higher powers**

Higher power levels are the most obvious method of increasing the limit from a single transistor.

Transistors may be paralleled. Precautions are taken to ensure that the devices should be matched. The devices should be matched on the same PCB.

Paralleling should be done on the collector but should not be done on the base. This implies using separate matching networks for the individual collector-to-collector connections. Common-emitter and collector-to-collector devices paralleled.

Push-pull operation becomes complicated at the equivalent parallel circuit to use with wideband operation is popular, particularly 70MHz.

Hybrid couplers in amplifier stages in series are identical in terms of Hybrid couplers have been eliminated from its construction. Solid-state vhf broad-band lines. There are suitable—hybrid couplers and the 3dB quadrature couplers may be connected to coaxial cable.

**Bias units for linear**

For ssb operation, a bias unit is required. 50-100mA. Low-impedance bias units are required. Figs 31 and 32. The power levels only. The bias must be greater than the amplifier stage.